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OVERVIEW

The last part of the project course deals with the control, assembling, and testing of the designed Dual Active Bridge (DAB) converter.

The regulation of the output voltage will be realised using a digital controller board (based on the Texas Instrument F28335 controller) developed by the laboratory. The controller is programmed in PLECS using so-called code generation, through which the model is compiled into C code before being loaded onto the microcontroller. The PLECS model generates pulse-width modulation signals to the switches according to a proportional-integral control loop. The gains of the control loop will first be tuned in offline simulations, similarly to the simulations in Report 1. Once the performance of the control loop has been validated offline, it will be integrated in the PLECS model that in turn is programmed onto the digital controller DSP. This model also implements all the necessary protection for safe operation of the converter during the subsequent testing.

Once the controller performance has been validated in simulations, the converter will be assembled and tested. To facilitate the debugging, each part of the converter will be tested systematically to step-by-step verify the correct behaviour of the converter.

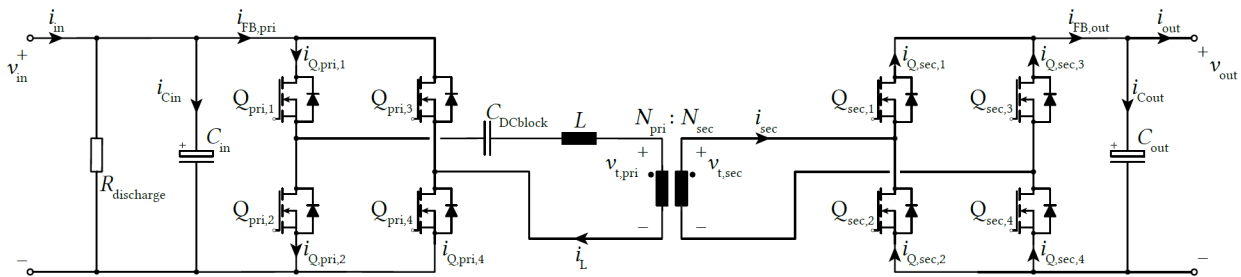


Figure 1 Schematics of the DAB converter for this report.

During the testing, the following instruments will be used:

- one digital controller,
- one BK Precision 9132B DC power supply,
- one BK Precision 8542B active load,
- one Rigol DS1074 oscilloscope,
- one Newtons4th Ltd PPA5530 power analyser,
- two current probes with amplifiers,
- and one FLIR E60 thermal camera

As in previous reports, please fill in the specifications assigned to your group in 1.

Table 1 Given parameters and design requirements for the DAB converter.

Property	Value	Unit
$P_{out,nom}$	50	W
$U_{in,nom}$	50	V
$U_{in,min}$	30	V
$U_{in,max}$	60	V
U_{out}	24	V
$\Delta U_{out,pp,rel}$	2	%
f_{sw}	250	kHz

SAFETY DISCLAIMER

The voltages and currents used during the testing of your converter can be sufficiently high to cause harm. Therefore, it is of outmost importance to respect safety precautions, by for example:

- Not touching any exposed connections when the converter is energised
- Always turning off the power before making any changes to the set up
- Using the available test points for measuring voltages in the converter. You should always make sure the probes are connected correctly with respect to ground before turning on the power. The voltage probes should be connected securely to the board, i.e. you should not hold the probe in place using your hands
- Using the current limit on the DC power supply by always setting it to a reasonable value. During the preliminary assembly and testing, it is recommended to keep the current limiter set to 0.1 A. Once the complete converter is tested, the current

limit should not be set higher than your expected RMS current. Setting the current limit appropriately will protect you, and the hardware components, in case of accidental short circuits

- Paying attention to polarity and pin order of components before soldering them to the PCB board
- Being careful when using the soldering irons, as these reach temperatures of close to 400°C

If in doubt, always ask.

INSTRUCTIONS ON REPORT STYLE

For the questions in this report, please provide descriptions of how each test or simulation was carried out. Include the details that are necessary to fully understand the setup or simulation. If the PCB needs to be modified, explain the reason for the modification. In case you cannot proceed with testing, explain what mistake is preventing you from proceeding and how the design could be improved if a second design iteration was allowed. Lastly, to ensure proper visualisation of the results, you are requested to export the waveforms of the oscilloscope using a USB stick. Failing to do so (e.g. taking pictures of the screen) could result in penalty points.

USAGE OF VOLTAGE PROBES

To measure voltages, either grounded or isolated measurements can be made. A grounded measurement is, as the name suggests, a measurement made between a given point and ground. This is different from an isolated measurement, where both nodes are floating and neither of them are connected to ground. Figure 2 shows the difference between grounded and isolated measurements. Isolated measurements must be performed using differential probes, in which both terminals are isolated from ground. These probes differ from single-ended probes, which can be used only for grounded measurements. Here, the ground of the instrument should be connected to the ground of your circuit using the ground terminal of the probe. Make sure to connect the probe close to the measurement point, especially if high frequencies are involved.

Be careful when connecting the probes to your test points. Make sure the ground connector of the probe is connected to ground at your test point to avoid short circuits. Connect the probes properly before energising the converter, and do not move them until you power it off. When measuring, always verify the attenuation factor of the probe.

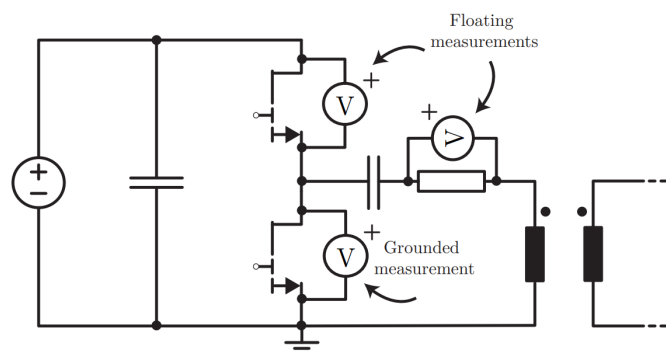


Figure 2 Example of grounded and isolated measurements.



Figure 3 Differential voltage probe (left) and single-ended voltage probe (right).

SOLDERING

A number of soldering stations will be set up in the laboratory for your usage. It is recommended to follow the structure of the report as opposed to solder many components at once, since some tests need to be performed without certain components soldered. After

you solder a component, check the continuity with a multimeter to look for unintentional short circuits or poor connections.

A quick guide to follow when soldering:

- For soldering the surface-mounted devices (SMDs), the temperature of the soldering irons should not exceed 380°C. It is allowed to set the temperature to a maximum of 400°C for soldering larger components on the PCB. This is the absolute maximum temperature, as tips of the iron risk getting damaged if they are too hot
- Regularly clean the tip with brass wool
- Do not push on the tip, as it is possible for them to break
- When soldering SMDs, tweezers can be used to hold the component in place. Avoid bad connections (so-called cold joints) by heating the copper pad of the PCB for a few seconds before applying the solder to it
- When removing a previously soldered component, use tweezers to carefully lift it from the copper pad while heating it up. Pulling on the component can cause the copper pad to detach from the PCB, and the copper trace to get damaged
- Please ensure that the soldering station is tidy and clean for the next user

IMPLEMENTATION OF DIGITAL CONTROL

For this part of the report, the given PLECS file `Digital_Control_Offline.plecs` will be used. Compared to the simulation files previously used in the course, the following changes can be observed:

- The generation of PWM signals is now dependent on the primary duty cycle `Duty_pri` and a phase shift reference `phi_timedelay_ref`, being the output of a proportional-integral control loop.
- The control scheme implements soft start in order to avoid large inrush currents at converter start-up. The duty cycle of the primary side is incrementally increased until the desired value of 0.5 is reached. At this point, the switching of the secondary side switches is enabled.
- Closed loop control of the output voltage is achieved using a proportional-integral control loop that acts on the difference between the measured output voltage and the reference voltage to produce a phase shift reference. Anti-windup is included to avoid windup of the integral term. This is important due to the needed saturation of the phase shift variable.
- The blocks `Vin setting` and `Rload setting` will be used to test the performance of the controller implementation. This is done by changing the input voltage and the load resistance (and thereby the output power) according to the profiles in Fig. 4 throughout the simulation.

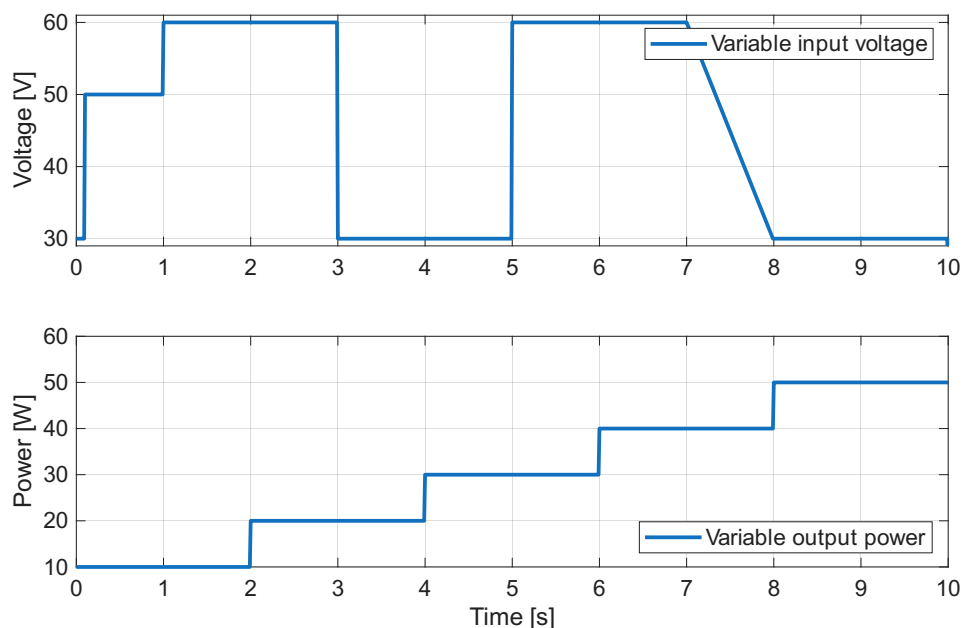


Figure 4 Voltage and power profiles for testing the controller implementation.

Q1: SOFT START IMPLEMENTATION

Complete the simulation model in `Digital_Controller_Offline.plecs` by including your own implementation of soft start inside the block `Soft start + primary side switching`. Include a screen shot of the implementation in the answer box below, as well as simulation results of how your variable `Duty_pri` increases at the start of the simulation.

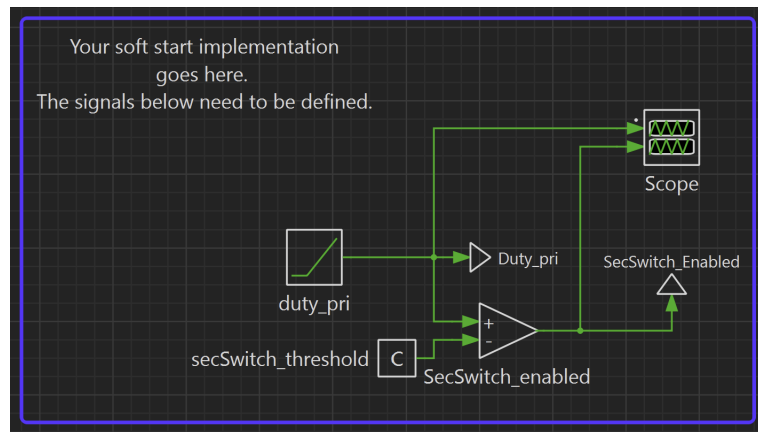


Figure 5 PLECS model of our implementation of the soft start

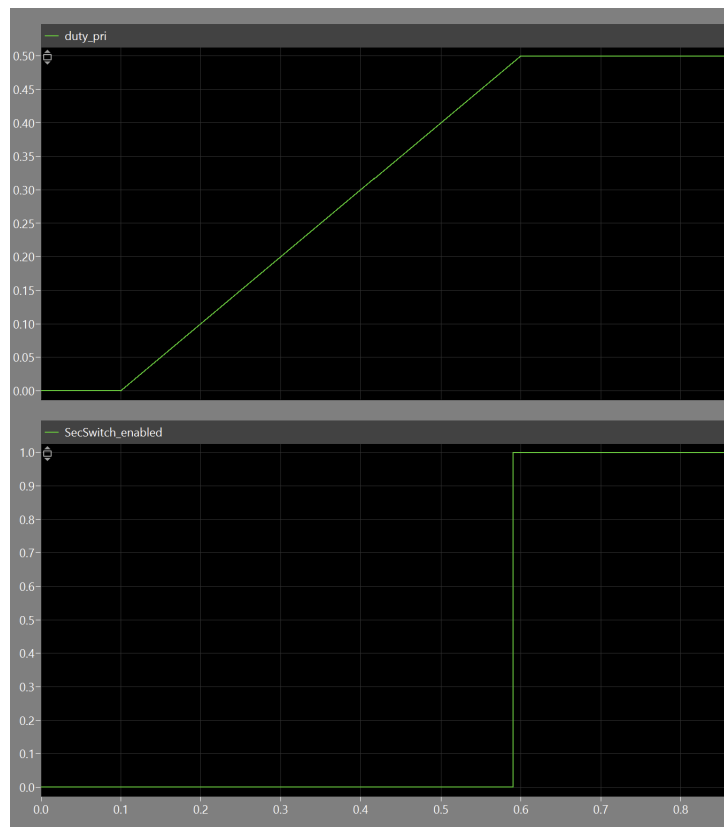


Figure 6 Figure of the implemented soft start. The first figure shows the ramping of the primary duty cycle. The second shows the switching on of the secondary when the primary reaches 0.5 duty cycle.

/ 2 pt.

Q2: DETERMINATION OF DEAD-TIME

A value of dead-time can be estimated from the data sheets of the switching devices and the gate driver. Referring to this application note, calculate the dead-time for your primary and secondary side switches. As the turn-on and turn-off delays depend on the gate driver design, we ask you to increase the safety margin to 1.5 as opposed to 1.2.

Based on the this application note, and increasing the safety margin to 1.5, we get that:

$$t_{dead} = [(t_{d,off,max} - t_{d,on,min}) + (t_{pdd,max} - t_{pdd,min})] \times 1.5$$

such that:

- t_{dead} : the calculated dead time.
- $t_{d,off,max}$ and $t_{d,on,min}$ are the turn-off and turn-on delay times.
- $t_{pdd,max}$ and $t_{pdd,min}$ represent propagation delay differences.

From the **PHP18NQ11T data sheet**, we get the following:

- $t_{d,off,max} = 18 \text{ ns}$
- $t_{d,on,min} = 6 \text{ ns}$

From the **UCC27288 data sheet**, we get the following:

- $t_{pdd,max} - t_{pdd,min} = t_{MON,max} = t_{MOFF,max} = 7 \text{ ns}$

We use this value since it quantifies the delay difference between the two gates signals.

Using these values we get:

$$t_{dead} = t_{d,pri} = t_{d,sec} = \left[(18 - 6) \times 10^{-9} + 7 \times 10^{-9} \right] \times 1.5 = 19 \times 10^{-9} \times 1.5 = 29 \times 10^{-9} \text{ s}$$

$$t_{d,pri} = 29 \text{ ns}$$

$$t_{d,sec} = 29 \text{ ns}$$

/ 2 pt.

Q3: DIGITAL CONTROL IN OPEN-LOOP

In your version of Digital_Controller_Offline.plecs, enable **Variable input voltage** and **Constant load** using the provided blocks, and run the simulation for your converter parameters and $V_{in,min}$. Define your calculated phase shift φ_{vmin} in the block **Generation of time delay (OL/CL setting)**, and run the simulation in open loop. Include a scope capture in the framed box below, and comment on the results. How is the system responding to the variation in input voltage?

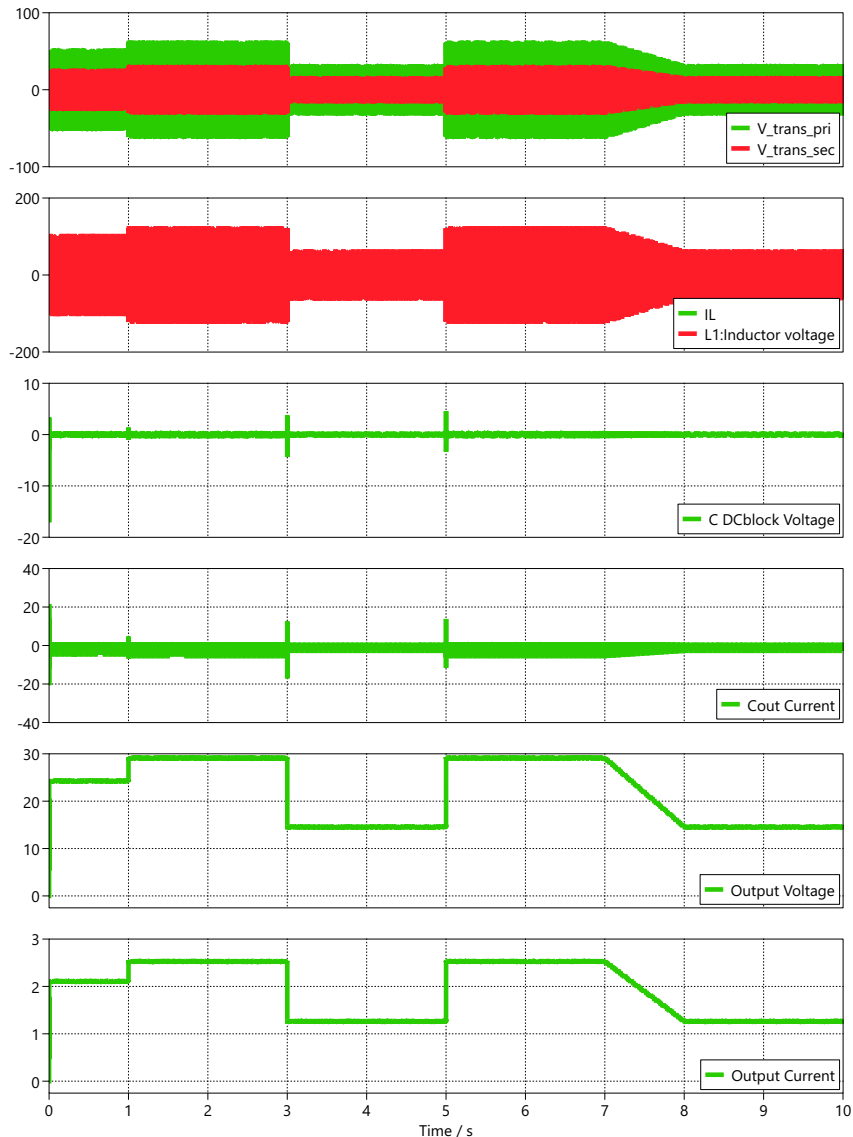


Figure 7 Waveforms of the open-loop simulation with variable voltage

We observe that we get the correct output voltage (24V) when the input is nominal (50V). But, for different input voltage, the output voltage varies proportionally to the input voltage. This is due to the fact that there is no control going on and the phase shift stays constant for all input voltage.

We also observe some current and voltage spikes when the input voltage changes rapidly (at 3s and 5s).

/ 4 pt.

Q4: DIGITAL CONTROL IN CLOSED-LOOP

You will now implement and run simulations for your digital controller. Enable closed-loop control by toggling the state of the switch inside the block **Generation of time delay (OL/CL setting)**. Complete the block **Controller with anti-windup** by providing the missing sampling times inside the zero-order hold blocks, saturation limits, and controller gains K_p , and K_i . Tune the controller gains until satisfactory performance is achieved, i.e. the output voltage is regulated to the desired level, despite variations in input voltage. As a final test, enable **Variable load** to check the performance during variable input voltage and variable load. Report the simulation results for the final controller gains, and comment on the results.

Note: There are several ways in which the performance of a controller implementation can be evaluated. In this task, we ask you to tune the controller gains so that the output voltage never deviates more than 10% from the desired value during transients (i.e. at the

points when input voltage or output power changes). Between these points, the output voltage should remain stable at the desired level. Clearly show that the requirements have been fulfilled using plots of your simulation results.

- **Zero-Order Hold sampling time:**

It is set equal to one switching period:

$$t_{ZOH} = \frac{1}{f_{sw}} = \frac{1}{250 \times 10^3} = 4 \mu s$$

- **Saturation limit:**

The values should at least include the min and max phase values of 0.236 and 0.524, found in report 1 (corresponding to 60V and 30V respectively). Setting the limits exactly to those values left no margin for the controller, causing the output voltage to saturate below or above 24 V during transients. After tuning, we selected a lower limit of 0.0 and an upper limit of 0.8 rad, providing approximately 0.25 rad of margin on each side of the operating range.

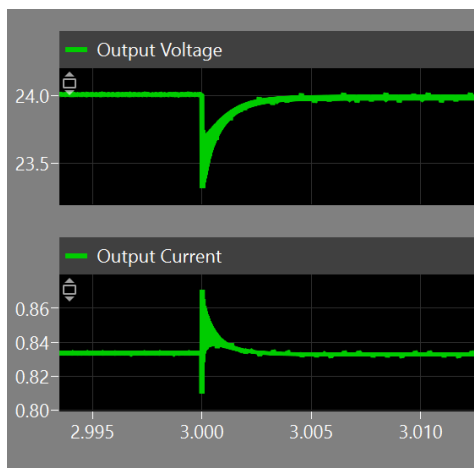
- **Controller gains:**

We started with random values of $K_p = K_i = 1$ and tuned them iteratively. We observed the following:

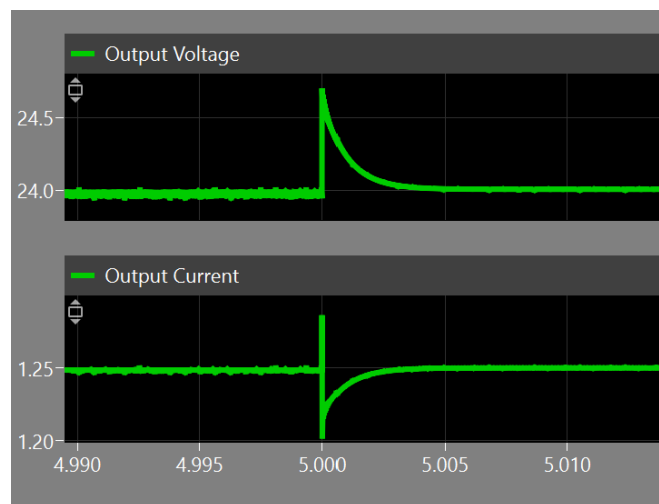
- For K_p : values over 0.4 lead to excessive oscillations of the output voltage. The final value is $K_p = 0.4$.
- For K_i : Increasing K_i reduces the recovery time after a sudden input voltage change, with limited negative impact on steady-state ripple. The final value is $K_i = 400$.

The main issue with the simulation was the sudden changes of input voltages at $t = 3$ s and $t = 5$ s (sudden steps between 60 V and 30 V input) that caused the output voltage to either increase above or decrease below the 10% allowed deviation (2.4 V in our case). After tuning the different values of K_p , K_i and the saturation limits, we got 23.3 V and 24.7 V output voltage values at $t = 3$ s and $t = 5$ s respectively, which are well inside of the 10% allowed margin of [21.6 ; 26.4]

One remaining issue occurs between $t = 1$ s and $t = 2$ s, when the input voltage is 60 V and the output power is 10 W. Under this condition, the output voltage rises slightly above the nominal 24 V. We are unsure of the origin of this behavior, but we discovered that allowing a negative phase shift (i.e. reverse power flow) would eliminate this discrepancy. Because bidirectional power flow is outside the scope of this design and this course, we decided to keep the lower saturation value at 0. The small steady-state overvoltage under this specific operating point is accepted in the scope of this class (after discussions with the TAs).



Output voltage peak value at 3s



Output voltage peak value at 5s



Output voltage stability between 0 and 1s



Output voltage stability between 6 and 7s

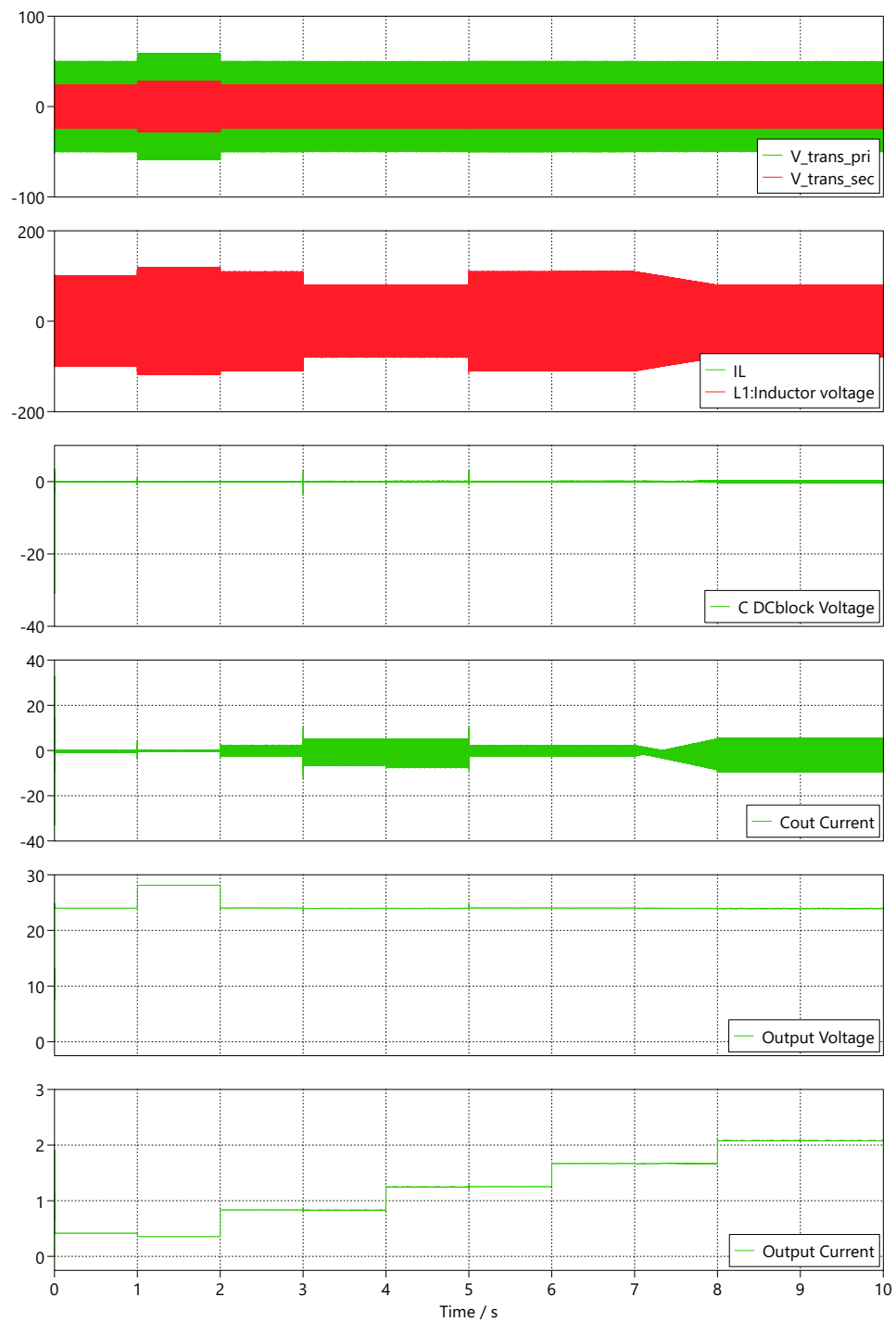


Figure 8 Waveforms with variable input and variable load

$t_{ZOH} = 4 \mu s$

Lower saturation limit = 0.0

Upper saturation limit = 0.8

$K_p = 0.4$

$K_i = 400$

/ 8 pt.

PRELIMINARY ASSEMBLY AND TESTING

Now that the digital controller is tuned and its performance has been tested, it is time to start the commissioning of the converter. In this section of the report, subsystems of the converter are assembled and tested one at a time. This initial assembly and testing do not involve any power transfer from the primary to the secondary side of the circuit.

SETTING UP THE DIGITAL CONTROLLER IN PLECS

The tests in this section require you to program the digital controller DSP using the provided PLECS model

Digital_Controller_Online.plecs. Configure it in the following way (settings are found by going to "Coder - Coder Options - Target").

- Set the target to "TI2833x"
- Set "Step size tolerance" to "Round to closest achievable value" (10% tolerance band)
- Set "Build configuration" to "Run from RAM"
- Set "Uniflash target configuration" to the path of the file TMS320F28335.ccxml on your laptops
- Finally, go to "Target - External Mode" to set "External Mode" to "Serial"

To program the digital controller, connect it to your laptop using a USB-C cable. Go to "Coder Options - External Mode" and set the target device to the correct COM port. Next, press "Build".

To observe ADC readings from the converter, go to "Coder Options - External mode" and press "Connect", followed by "Active autotriggering". Now, scopes and displays in the PLECS model will update in real time.

Q5: VERIFICATION OF PRIMARY AUXILIARY POWER SUPPLY

Solder the main input connector, along with all the components associated with the primary auxiliary power supply. Using the DC power supply (pay attention to the polarity of the connector) and an oscilloscope connected to the test points of interest, verify that the voltages are correctly regulated to 12 V and 3.3 V. Include an oscilloscope capture in the framed box below.

The pictures bellow show that the voltages are regulated at the correct values.



/ 4 pt.

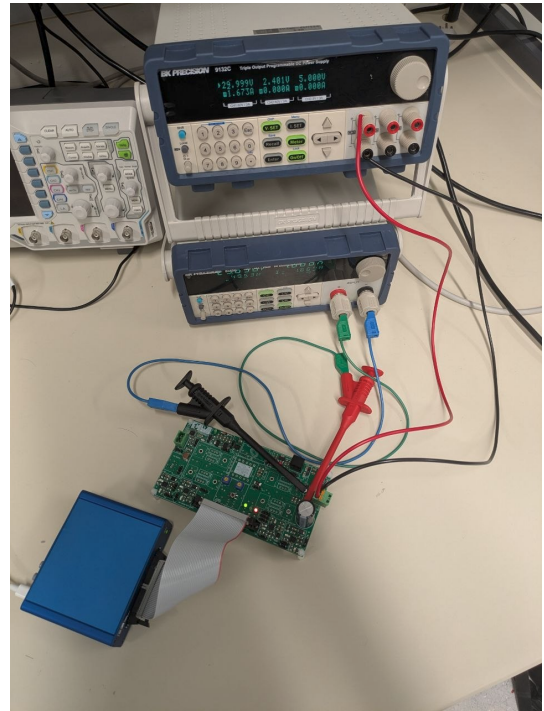
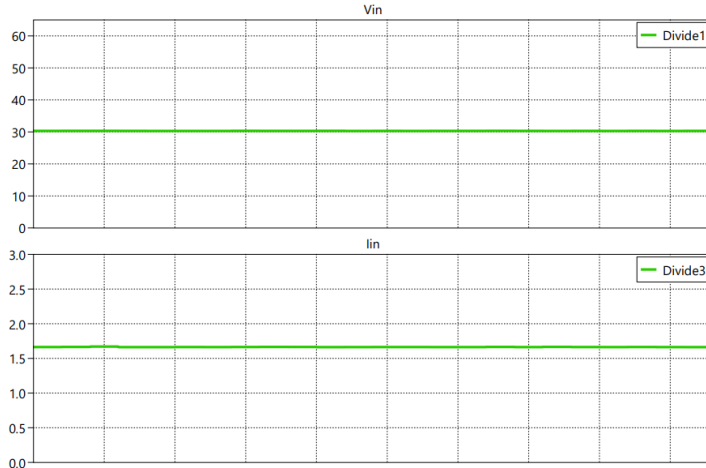
Q6: VERIFICATION OF PRIMARY SENSING CIRCUIT

Solder the shunt resistor, and all the components belonging to the primary sensing circuit. In addition, solder the connector for the digital controller. Using the appropriate test points, connect a variable resistor in series with the shunt resistor, i.e. between the shunt resistor and ground on the PCB. This provides a path for the current to flow from the positive terminal to the negative terminal of the DC power supply. Using the variable resistor and the DC power supply, set V_{in} to obtain the rated current for which the shunt resistor was sized. Open Digital_Controller_Online.plecs, update the simulation parameters with your values, build the model, and connect to the digital controller. Ensure that the scaling of the incoming ADC signals is correct, and that the expected values of V_{in} and I_{in} are obtained. In the framed box below, show a picture of your measurement set up, and your ADC readings from PLECS.

To verify the primary sensing circuit, the shunt resistor ($R_{shunt,pri} = 25\text{ m}\Omega$) and all primary sensing components were soldered, along with the digital controller connector.

The rated current for the primary shunt was sized at $I_{in,max} = P_{out}/V_{in,min} = 50/30 = 1.667\text{ A}$. To reproduce this condition, the DC power supply was set to $V_{in} = 30\text{ V}$ and the DC electronic load was configured in constant current (CC) mode at $I = 1.667\text{ A}$.

The PLECS model was built and connected to the DSP. As shown in the PLECS screenshot, the ADC readings for V_{in} and I_{in} match the expected values closely, confirming correct scaling of the sensing circuit. No further calibration was required.



Measurement set up : power supply set to 30V and load set to current control mode with a current set at 1.667A

/ 3 pt.

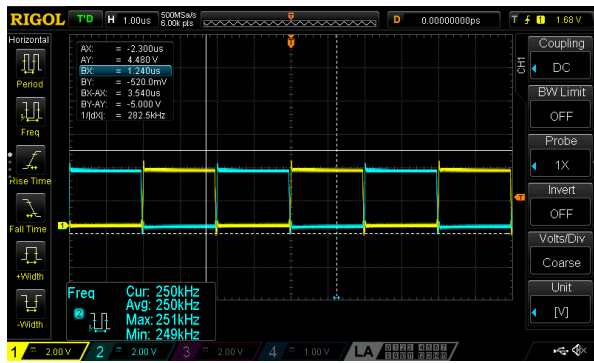
Q7: VERIFICATION OF PRIMARY SIDE GATE DRIVERS

Solder all components that make up the primary side gate drivers. The actual MOSFETs will be soldered at a later stage. Use the provided PLECS model to generate PWM signals for the primary switches. To do so, the fault thresholds defined in the **Protection** block may need to be changed, as no PWM signals will be generated as long as the controller is in fault state. In the framed box below, include an oscilloscope capture of the PWM signals received from the digital controller and measure the generated dead-time using cursors. Confirm that the value of dead-time is as expected. In addition, include an oscilloscope capture to show the gate signals of the two low-side devices on the primary side.

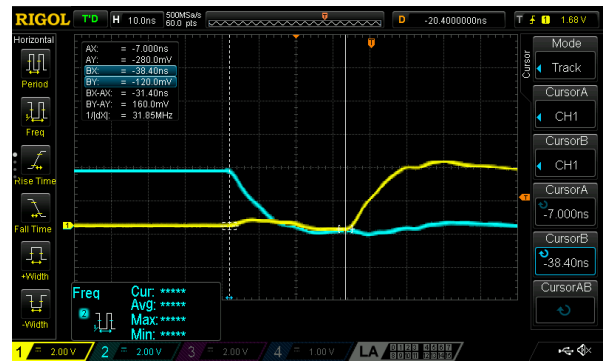
Since the internal clock frequency is set to 150 MHz, the smallest time step resolution is $t_{res} = \frac{1}{150 \times 10^6} \approx 6.67\text{ ns}$. As the computed dead time was $t_{dead} = 29\text{ ns}$, the DSP rounds this to the nearest possible multiple: $5 \times t_{res} \approx 33\text{ ns}$.

To generate PWM signals without triggering fault state, some of the **Protection** values were changed to allow a normal functioning of the DSP.

The results are shown below:



PWM1A (Blue) and PWM1B (Yellow): full period view



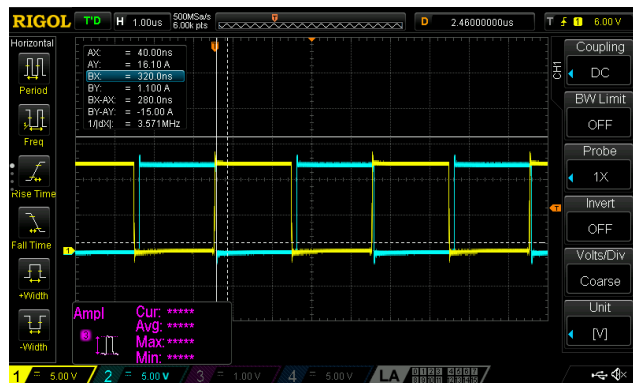
PWM1A (Blue) and PWM1B (Yellow): dead-time zoomed view

The cursor measurement on the zoomed capture confirms a dead-time of $t_{dead,measured} = 31.4 \text{ ns}$, which is consistent with the expected $5 \times t_{res} \approx 33 \text{ ns}$ given the DSP clock.

The board was then powered at $V_{in} = 30 \text{ V}$ with the current limit set to 0.1 A.

The gate signals of the two primary low-side MOSFETs (G2P and G4P) were measured at the low-side gate driver outputs.

As seen in the picture, both signals swing between 0 V and 12 V as expected, confirming correct operation of the UCC27288. The high-side gate signals were not verified at this stage, as the bootstrap capacitor cannot charge without the MOSFETs soldered.



G4P (Blue) and G2P (Yellow): full period view

/ 6 pt.

Q8: VERIFICATION OF PRIMARY SIDE MOSFET OPERATION

Solder the primary side MOSFETs, and pay attention to the order of the pins. The heatsinks do not need to be mounted at this point. However, make sure that the height at which the MOSFETs are soldered makes it possible to attach them to the chosen heatsinks later on. With the input voltage set to 30 V, use the test points to measure the drain-source voltages of the low-side MOSFETs. In the framed box below, insert a picture of your oscilloscope capture. Comment on how your chosen value of dead-time is performing.

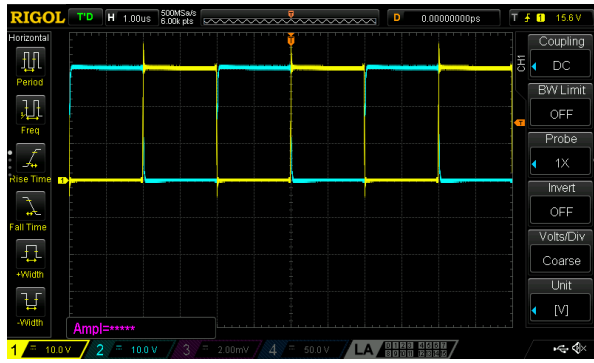
Note: Set the current limit of the DC power supply to 0.1 A. This is to avoid issues with shoot-through in case the chosen value of dead-time is too short.

Note 2: A useful application note on MOSFET operation can be found [here](#).

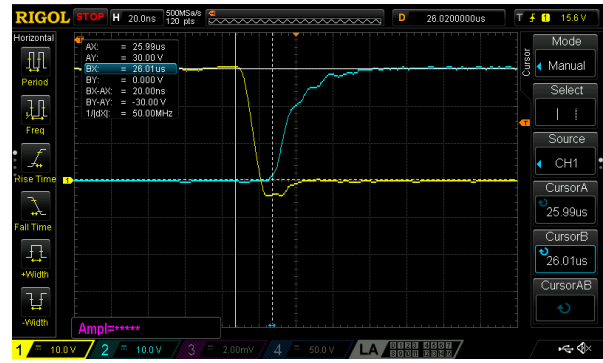
The four primary side MOSFETs (PHP18NQ11T) were soldered, ensuring correct pin orientation and sufficient height above the PCB to allow heatsink attachment later. The input voltage was set to $V_{in} = 30 \text{ V}$ with the current limit set to 0.1 A.

Remark: In our testing timeline, this test, and the primary side MOSFET soldering, were the second last (right before the secondary side MOSFET soldering and testing) steps performed before soldering the transformer and inductor.

The drain-source voltages of the two primary low-side MOSFETs (Q2 and Q4) were measured simultaneously using two oscilloscope probes connected to the corresponding test points. The results are shown in the pictures below:



Picture 1: $V_{DS,Q2p}$ (Yellow) and $V_{DS,Q4p}$ (Blue): full period view.
Both signals alternate correctly between 0 V and 30 V at $f_{sw} = 250$ kHz.



Picture 2: $V_{DS,Q2p}$ (Yellow) and $V_{DS,Q4p}$ (Blue): zoomed view at 20 ns/div showing the switching transition. Cursor measurement: $t_{dead,measured} \approx 20$ ns.

Comments on dead-time performance:

The cursor measurement on Picture 2 gives $t_{dead,measured} = 20$ ns, which is slightly lower than the expected $5 \times t_{res} \approx 33$ ns. This difference may be due to cursor placement uncertainty at this timescale.

No overcurrent event was observed during the test (the 0.1 A current limit on the supply was never triggered), confirming the absence of shoot-through.

/ 6 pt.

Q9: VERIFICATION OF INDUCTOR OVER-CURRENT CIRCUIT

The inductor over-current circuit will be tested in a similar way to Q6. Start by soldering all components related to the protective circuit, including the three LEDs that are connected to the digital controller outputs. Connect a variable resistor in series with the shunt resistor for the measurement. Determine the necessary input voltage to obtain the peak current used for the sizing of the shunt resistor in Report 3. The PWM signals in the PLECS model will need to be altered to have a consistent current loop, as switch 4 (refer to Fig 1) needs to be gated on for the entire test, while the other switches should be gated off. Once the peak current is obtained, tune both potentiometers at the same time to trigger the over-current protection. This should turn on the red LED on the PCB. In the framed box below, include a picture of the measurement set up, and state the current threshold at which the protection is triggered.

Note: Given the test set-up, it is not possible to obtain a negative current through the shunt resistor with which the second potentiometer can be tuned. To overcome this limitation, we ask you to tune the potentiometers to approximately the same resistance value.

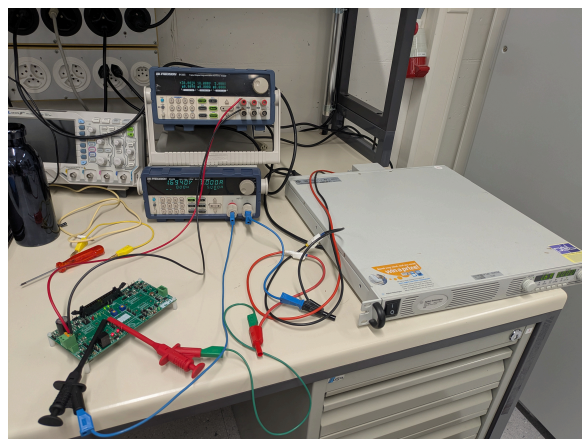
All components related to the inductor over-current protection circuit were soldered, including the three LEDs connected to the digital controller outputs. The DC electronic load was used in place of a variable resistor, configured in constant current (CC) mode for precise current control.

The test circuit was set up as follows:

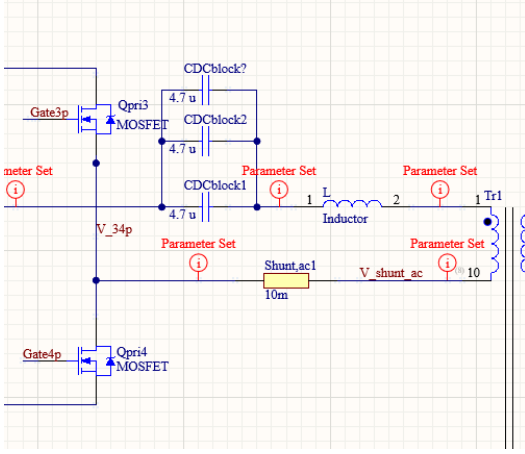
The node V_{34p} was connected to the DC supply at a test voltage V_{test} , while the ground reference was placed at the output of the AC shunt ($V_{shunt,ac}$), placing the shunt and the load in series between the supply and ground (see pictures below).

There was no need to switch ON the gates in PLECS since at that moment, our transistors were not soldered yet so that the imposed voltage bypassed that problem.

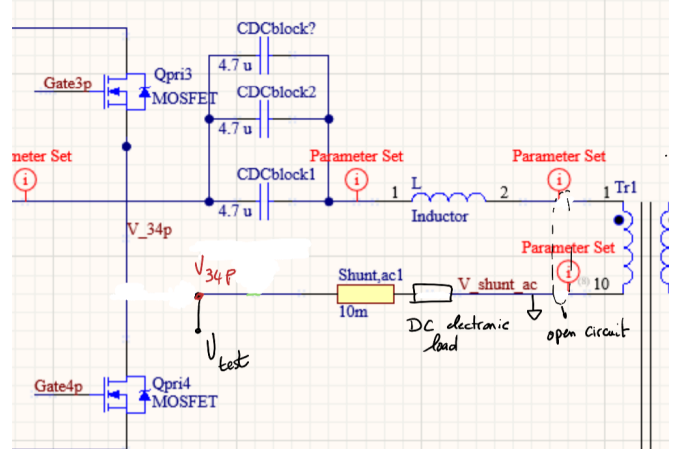
The load was first set to $I = I_{L,peak} = 3.6$ A to verify the current path, then increased toward the target threshold $I_{th,design} = 1.4 \times 3.6 = 5.04$ A.



Measurement set up : power supply capable of outputting 5A set to 1.67V (since we don't care about the voltage) and load set to current control mode with a current set at 5A



Schematics view



Explanation of the setup using the electronic load.

Component adjustment:

During testing, it was found that the original fixed resistor $R_{div,1, fixed} = 25.5 \text{ k}\Omega$ (in series with the $10 \text{ k}\Omega$ potentiometer) did not allow the protection to be triggered at the intended threshold. The minimum achievable threshold with the potentiometer at maximum resistance was insufficient to reach 5.04 A . The fixed resistor was therefore replaced by $R_{div,1, fixed} = 43.3 \text{ k}\Omega$, and by tuning the potentiometer, we shifted the threshold to the desired value of 5 A .

The test was realized for both potentiometer, since with our setup, it was possible to test both potentiometer simply by inverting the V_{test} and GND.

$$I_{th} = 5 \text{ A}$$

/ 3 pt.

Q10: VERIFICATION OF DISCHARGE RESISTOR

Solder the input capacitors, and the discharge resistor. Ensure that the polarity of any electrolytic capacitor used is respected. Using the DC power supply and an oscilloscope connected to the relevant test points, capture the discharging waveform similarly to the dummy picture below. Report the time it takes for the capacitors to discharge, and comment on the results.

Note: Consider using the "ROLL" setting to capture the discharging waveform on the oscilloscope. It can be found under "Horizontal - Menu - Time base" by changing from "YT" to "ROLL".

The input capacitors and discharge resistor were soldered.

The total input capacitance is:

$$C_{total} = C_{elec} + C_{cer} = 680 \mu\text{F} + 2 \times 4.7 \mu\text{F} = 689.4 \mu\text{F}$$

The oscilloscope was connected between the V_{in} test point and GND, and the time base was set to ROLL mode at 2 s/div .

The input voltage was set to $V_{in} = 60 \text{ V}$ to maximize the discharge time (worst case). Two discharge methods were compared:

1. Method 1: Power supply turned off:

The internal resistance of the DC power supply was measured at $R_{supply} \approx 2.8 \text{ k}\Omega$, which appears in parallel with the discharge resistor during discharge. The effective resistance is:

$$R_{eff,1} = R_{dis} || R_{supply} = \frac{28.7 \text{ k}\Omega \times 2.8 \text{ k}\Omega}{28.7 \text{ k}\Omega + 2.8 \text{ k}\Omega} = 2.55 \text{ k}\Omega$$

$$\tau_1 = R_{eff,1} \times C_{total} = 2550 \times 689.4 \times 10^{-6} \approx 1.76 \text{ s}$$

$$t_{discharge,1} = 5\tau_1 \approx 8.8 \text{ s}$$

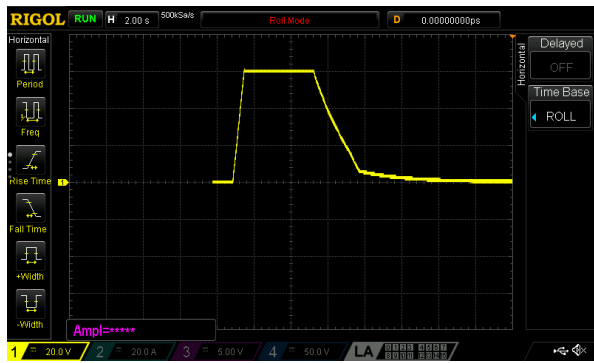
2. Method 2: Input cable disconnected:

Disconnecting the cable removes the supply's internal resistance from the discharge path, leaving only the discharge resistor.

This results in a longer time constant:

$$\tau_2 = R_{dis} \times C_{total} = 28.7 \times 10^3 \times 689.4 \times 10^{-6} \approx 19.8 \text{ s}$$

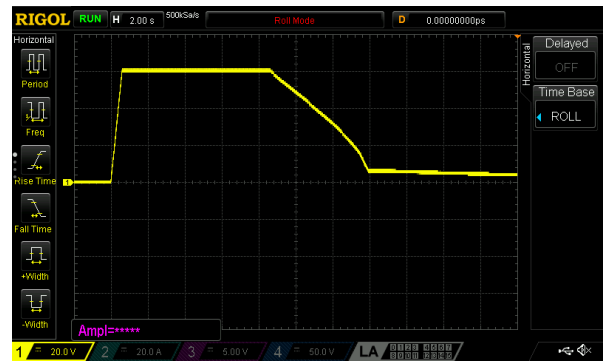
$$t_{discharge,2} = 5\tau_2 \approx 99 \text{ s}$$



Method 1: discharge with power supply turned off. The measured discharge time is $t_{\text{discharge},1} \approx 10$ s, consistent with $5\tau_1 \approx 8.8$ s.

Method 1 is faster because the supply's internal resistance (2.8 k Ω) provides an additional discharge path in parallel with the discharge resistor, effectively reducing the time constant from 19.65 s to 1.75 s.

Method 2 represents the true worst-case discharge scenario, confirming that the capacitors discharge fully within approximately 99 s (≈ 1.6 min) through the 28.7 k Ω resistor alone, which satisfies the safety requirement.



Method 2: discharge with cable disconnected. The decay is significantly slower, and the full discharge extends well the 20 s oscilloscope window, consistent with $5\tau_2 \approx 99$ s.

/ 5 pt.

Q11: VERIFICATION OF SECONDARY AUXILIARY POWER SUPPLY

As the correct operation of the subsystems on the primary side have now been verified, it is time to verify the corresponding subsystems on the secondary side. Omitting the DC blocking capacitors, inductor, and transformer for now, 18 V will be supplied to the auxiliary circuit of the secondary side using the appropriate test point and the DC power supply. Note that the primary side does not need to be energised for this part of the report. Solder the output connector, along with all components associated with the secondary auxiliary power supply. Using a DC power supply and an oscilloscope connected to the test points of interest, verify that the voltages are correctly regulated to 12 V and 3.3 V. Please include your own oscilloscope captures in place of the dummy figure.

A voltage of 18 V was supplied to the board via the test points. The results below show that the voltages are regulated at the correct values of 3.3 V and 12 V and is stable.



3V3 regulated voltage

12V regulated voltage

/ 4 pt.

Q12: VERIFICATION OF SECONDARY SENSING CIRCUIT

Solder the shunt resistor used for the DC current measurement on the secondary side, along with all components belonging to the secondary sensing circuits. Using the appropriate test points, connect a variable resistor in series with the shunt resistor, thereby providing a path for the current to flow from V_{out} to ground. Using the resistor value and DC power supply, set V_{out} to obtain the rated current for which the shunt resistor was sized. Ensure that the scaling of the incoming ADC signals are correct, and that the expected

values of V_{out} and I_{out} are obtained. In the framed box below, show a picture of your measurement set up, and your ADC readings from PLECS.

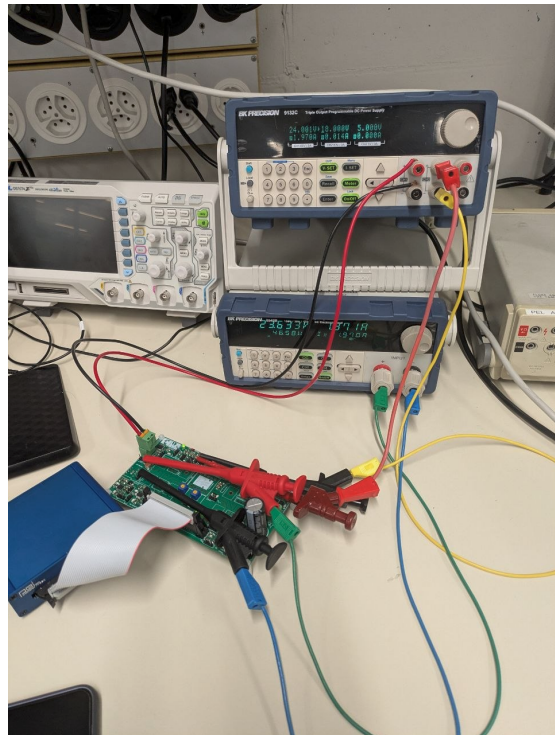
To verify the secondary sensing circuit, the output shunt resistor ($R_{shunt,sec} = 20\text{ m}\Omega$) and all secondary sensing components were soldered.

The rated current for the secondary shunt was sized at $I_{out,max} = P_{out}/V_{out} = 50/24 = 2.083\text{ A}$.

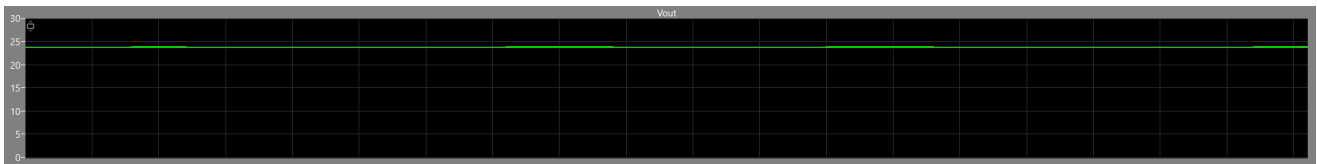
The DC power supply was set to $V_{out} = 24\text{ V}$ and the DC electronic load was configured in constant current (CC) mode at $I = 2.083\text{ A}$.

As the sensing circuit cannot measure a backward flowing current, in order to perform the measurements of I_{out} , we imposed a voltage of -24 V through the output pin to reverse the direction of the current through the shunt resistor and allow its measurements.

The ADC readings shown in the PLECS screenshots match the expected values closely, confirming correct values for both V_{out} and I_{out} . No further calibration was required.



Measurement set up : power supply set to 24V and load set to current control mode with a current set at 2A



V_{out} measured with the output voltage set at 24V.



I_{out} measured by setting the output voltage at -24 V (to allow a forward current through the sensing circuit)

/ 3 pt.

Q13: VERIFICATION OF SECONDARY SIDE GATE DRIVERS

Solder all components that make up the secondary side gate drivers. The actual MOSFETs will be soldered at a later stage. Use the PLECS model to generate PWM signals for the secondary side. To do so, the fault thresholds defined in the **Protection** block may need to be changed. In the framed box below, include an oscilloscope capture of the PWM signals received from the digital controller and measure the generated dead-time using cursors. Confirm that the value of dead-time is as expected. In addition, include an oscilloscope capture to show the gate signals of the two low-side devices on the secondary side. Finally, provide an oscilloscope capture showing the phase shift between PWM signals on the primary and those of the secondary. Does it correspond to the desired value?

Note: The provided PLECS model includes the option to manually set the phase shift, rather than using the output of the closed-loop control. This setting is found in the block **Generation of time delay (pu)**.

All secondary side gate driver components were soldered without the MOSFETs. As for the primary side, the relevant **Protection** thresholds were modified to allow normal DSP operation. The phase shift was set manually in the block **Generation of time**

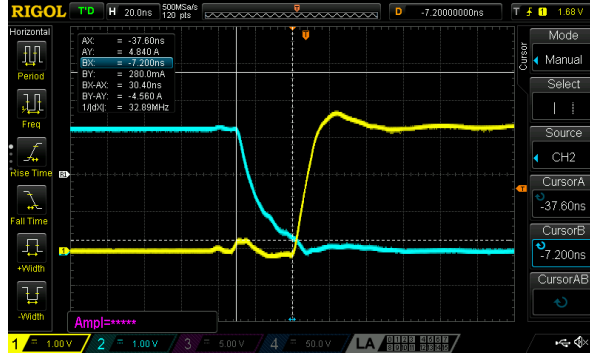
delay (pu) to two values: $\varphi = 0.4$ and $\varphi = \pi/2$.

Dead-time measurement (Picture 1):

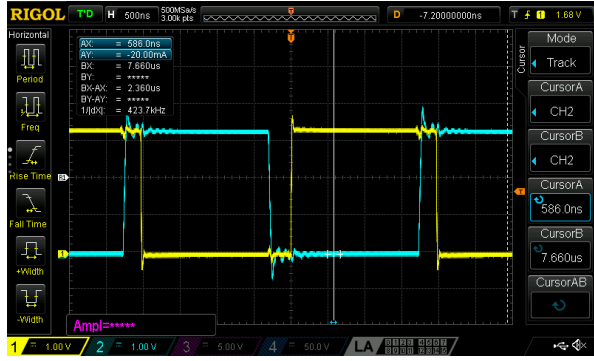
The same clock quantization applies as on the primary side: $t_{dead,expected} = 5 \times t_{res} \approx 33$ ns. The cursor measurement confirms:

$$t_{dead,measured} = 30.40 \text{ ns} \approx 33 \text{ ns}$$

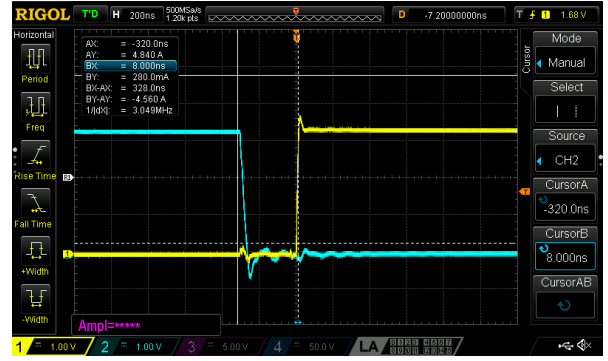
This is consistent with the primary side result and with the expected DSP clock quantization to $5 \times t_{res}$.



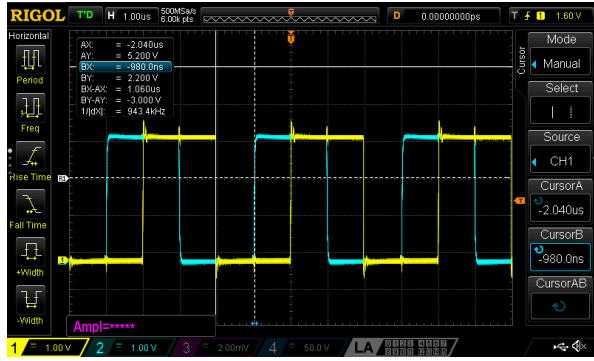
Picture 1: Dead-time measurement using cursors on the secondary side PWM signals (Yellow = PWM3B / Blue = PWM3A)



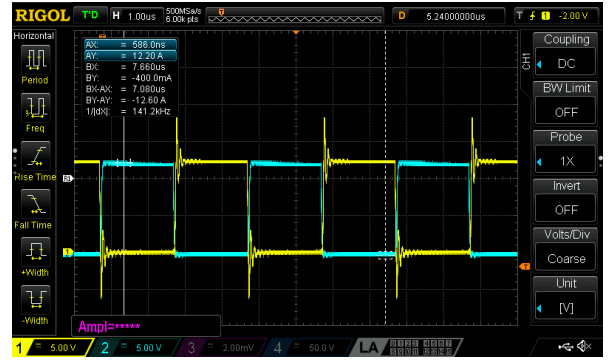
Picture 2: Primary PWM1A (Blue) vs secondary PWM3B (Yellow) with a phase shift of $\varphi = 0.4$ rad: full period view



Picture 3: Primary PWM1A (Blue) vs secondary PWM3B (Yellow) with a phase shift of $\varphi = 0.4$ rad: Cursor measures



Picture 4: Primary PWM1A (Yellow) vs secondary PWM3B (Blue) with a phase shift of $\varphi = \pi/2$ rad: Cursor measures.



Picture 5: Secondary low-side gate driver outputs G4S (Yellow) and G2S (Blue): full period view

Phase shift verification: The expected time delay between primary and secondary PWM is as follows:

- For $\varphi = 0.4$ rad, the expected time delay between primary and secondary PWM is:

$$\Delta t_{expected} = \frac{\varphi}{2\pi \times f_{sw}} = \frac{0.4}{2\pi \times 250 \times 10^3} = \frac{0.4}{1.571 \times 10^6} \approx 0.26 \mu s$$

This value is confirmed by **picture 3** that shows a phase shift of $0.3 \mu s \approx 0.26 \mu s$.

- For $\varphi = 1.57$ rad:

$$\Delta t_{expected} = \frac{\varphi}{2\pi \times f_{sw}} = \frac{1.57}{2\pi \times 250 \times 10^3} = \frac{1.57}{1.571 \times 10^6} = 1.0 \mu s$$

This value is confirmed by **picture 4** that shows a phase shift of $1.06 \mu s \approx 1 \mu s$.

The secondary low-side gate signals (**Picture 5**) swing between 0 V and 12 V at 250 kHz (1 period = $4 \mu\text{s} \Rightarrow f = \frac{1}{4 \times 10^{-6}} = 250 \times 10^3 \text{ Hz}$), confirming correct UCC27288 operation.
The high-side gate signals were not verified at this stage as the bootstrap capacitor cannot charge without the MOSFETs soldered.

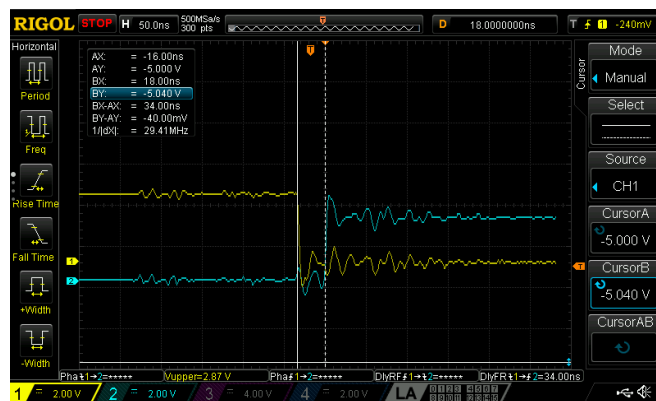
/ 6 pt.

Q14: VERIFICATION OF SECONDARY SIDE MOSFET OPERATION

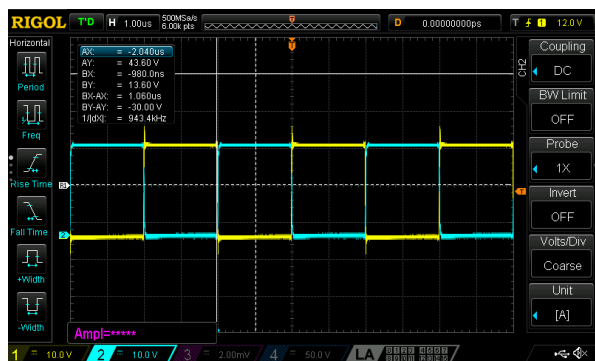
Solder the secondary side MOSFETs, and pay attention to the order of the pins. The heatsinks do not need to be mounted at this point. However, make sure that the height at which the MOSFETs are soldered makes it possible to attach them to the chosen heatsinks later on. With the output voltage set to the desired level, use the test points to measure the drain-source voltages of the low-side MOSFETs. In the framed box below, insert a picture of your oscilloscope capture. Comment on how your chosen value of dead-time is performing.

Note: Set the current limit of the DC power supply to 0.1 A. This is to avoid issues with shoot-through in case the chosen value of dead-time is too short.

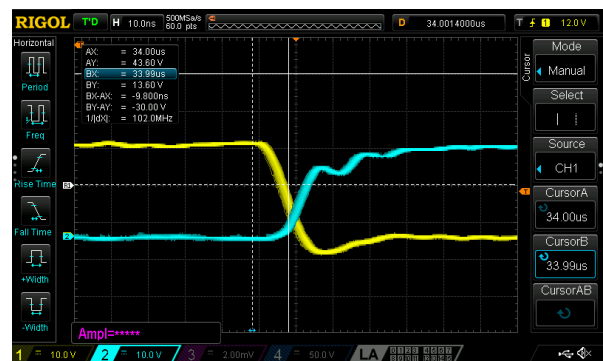
The four secondary side MOSFETs (PHP18NQ11T) were soldered, ensuring correct pin orientation and sufficient height above the PCB to allow heatsink attachment later. The output voltage was set to $V_{out} = 24 \text{ V}$ with the current limit set to 0.1 A. The PWM were checked to verify the dead time as seen in picture 1.



Picture 1: Dead time measurement on the PWM3A and PWM3B. The value of the observed dead time is indeed of 34 ns. The drain-source voltages of the two secondary low-side MOSFETs (Q2S and Q4S) were measured simultaneously using two oscilloscope probes connected to the corresponding test points).



Picture 2: $V_{DS,Q2S}$ (Yellow) and $V_{DS,Q4S}$ (Blue): full period view.
Both signals alternate correctly between 0 V and 24 V at $f_{sw} = 250 \text{ kHz}$.



Picture 3: $V_{DS,Q2S}$ (Yellow) and $V_{DS,Q4S}$ (Blue): zoomed view showing the switching transition. No overlapping of the waveforms, confirming absence of shoot-through.

Comment on an encountered issue :

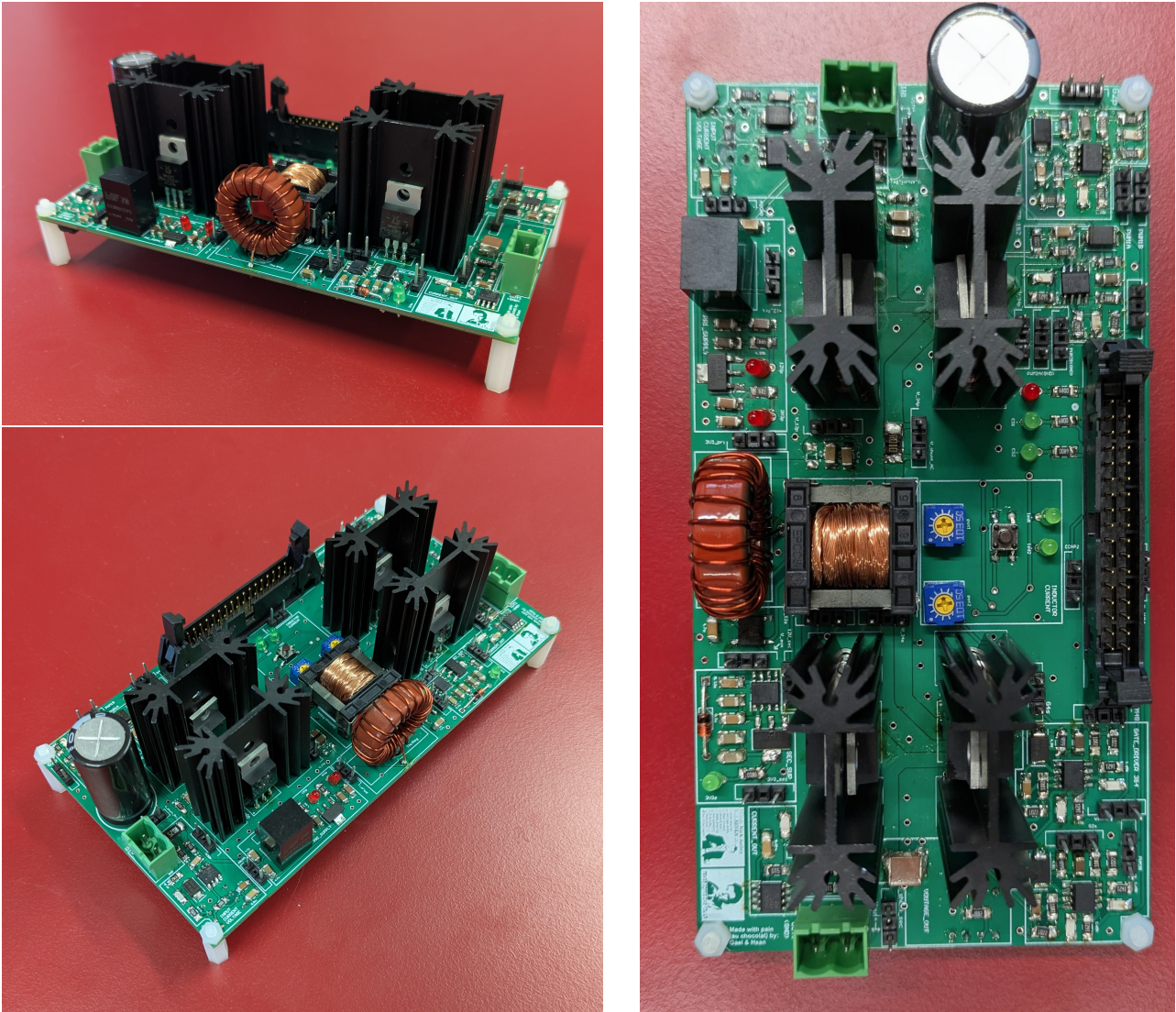
While proceeding with this test, we found that the power supply shorted when turned on. At first, we could not understand why this was happening. We initially observed that the issue only occurred when the controller was operating. We also noticed that one of the MOSFETs would not switch, so we decided to replace it, which turned out to be quite a long process. However, this did not solve the issue.

We then modified the PLECS model to enable switching on either the 3rd or 4th gate driver only, and found that the short circuit occurred only when the 4th gate driver was enabled. We therefore observed the output of the gate driver and found that it had a strange waveform. It turned out to be a bad solder joint on the gate driver. Resoldering it solved the issue.

COMPLETING THE CIRCUIT AND OPEN-LOOP OPERATION

Q15: FINAL ASSEMBLY OF CONVERTER

Solder the inductor, DC blocking capacitors, transformer, diode rectifier, and Zener diode. The Zener diode needs to be soldered (respecting the polarity) across the output pins of the diode rectifier to protect the linear voltage regulator against over-voltages. Attach the MOSFETs to heatsinks according to your design, not forgetting the TIM sheet. In the framed box below, include a picture of your converter with all components soldered.



In this picture, the heatsinks have only been placed temporarily (without being fixed to the MOSFETs). The TIM sheets and nylon screw were added later during the tests. Moreover, after conducting all of the tests, specifically the heat tests, we decided to remove the primary side heat sinks because the temperature in that side was low enough.

Q16: TESTING OF OVER-VOLTAGE AND OVER-CURRENT PROTECTION

To ensure that the implemented protection works as intended, the detection of over-voltage and over-current will be tested. The digital controller is made to stop PWM as soon as fault state is entered, meaning that any triggering of over-voltage or over-current is visible by monitoring the PWM signals received from the controller.

Validate the activation of over-voltage protection for the primary side by setting the trigger threshold to a value lower than the intended threshold value. Measure any of the primary side PWM signals received from the digital controller, as well as the input voltage. Report the oscilloscope capture at the point when the over-voltage protection triggers. Also, measure the input voltage level at this point using cursors. Repeat the procedure to validate the correct operation of the over-current detection.

In the framed box below, insert the oscilloscope captures that show the activation of over-voltage and over-current protection on the primary and secondary side. Make sure to explain how the tests were carried out, for instance by stating what the threshold values were set to.

Note: To trigger the oscilloscope at the point where the PWM signal is stopped by the digital controller, consider using the trigger type called "Timeout".

The oscilloscope was configured in **Timeout** trigger mode on the PWM signal to capture the moment the DSP stops switching for all the tests below.

Primary over-voltage protection:

The primary over-voltage threshold was temporarily lowered to $V_{in,OV} = 40$ V. The input voltage was increased from 38 V until the threshold was crossed. At $V_{in} \approx 40$ V, the DSP entered fault state and PWM1A stopped, as shown in Picture 1.

Secondary over-voltage protection:

The secondary over-voltage threshold was temporarily lowered to $V_{out,OV} = 22$ V. The output voltage was increased from 20 V. The oscilloscope capture showed a result similar to the previous case.

Primary over-current protection:

Using the same setup as Q6 (electronic load in CC mode on the primary shunt), the over-current threshold was lowered to $I_{in,OC} = 1.5$ A. The current was slowly increased from 1 A. At $I_{in} \approx 1.5$ A, the PWM stopped as shown in Picture 2.

Secondary over-current protection:

Using the same setup as Q12 (electronic load in CC mode with reversed voltage for correct current direction through the secondary shunt), the threshold was lowered to $I_{out,OC} = 2$ A. The current was increased from 1.5 A. At $I_{out} \approx 2$ A. The result was similar to the previous case.

From the pictures below, we observe that the protection worked properly and that the PWM was switched off.



Picture 1: PWM1A during overvoltage detection.

Picture 2: PWM1A during overcurrent detection.

During this testing, we found that the inductor over current detection was always triggering despite the threshold being correctly configured at 5 A, well above the expected maximum inductor current of 3.6 A. After investigation, we concluded that some current spikes were the cause of this issues, and after (hours of) debugging, we decided to simply turn of the inductor over current fault, and everything worked fine from that point on.

/ 6 pt.

Q17: TESTING OF SOFT START IMPLEMENTATION

An implementation of soft start is already included in the provided PLECS model. Verify its correct operation by using an oscilloscope to measure a PWM signal at converter start up, together with the drain-source voltage of one of the primary side switches. Insert your oscilloscope capture, and comment on the results in the framed box below. How come the drain-source voltage only appears after a number of switching cycles?

The soft start implementation was verified by measuring simultaneously a primary PWM signal and the drain-source voltage of one of the primary side low-side MOSFETs at converter start-up. This is shown in the picture bellow. We can see that the drain-source voltage only begins switching after a number of PWM cycles. This delay is a direct consequence of the soft start sequence

implemented in the **Soft start + primary side switching** block: the primary duty cycle **Duty_pri** is incrementally ramped from 0 to 0.5 before the secondary side switching is enabled. During this ramp-up phase, the duty cycle is too short for the MOSEFTs to turn thus the absence of the V_{DS} during that period.

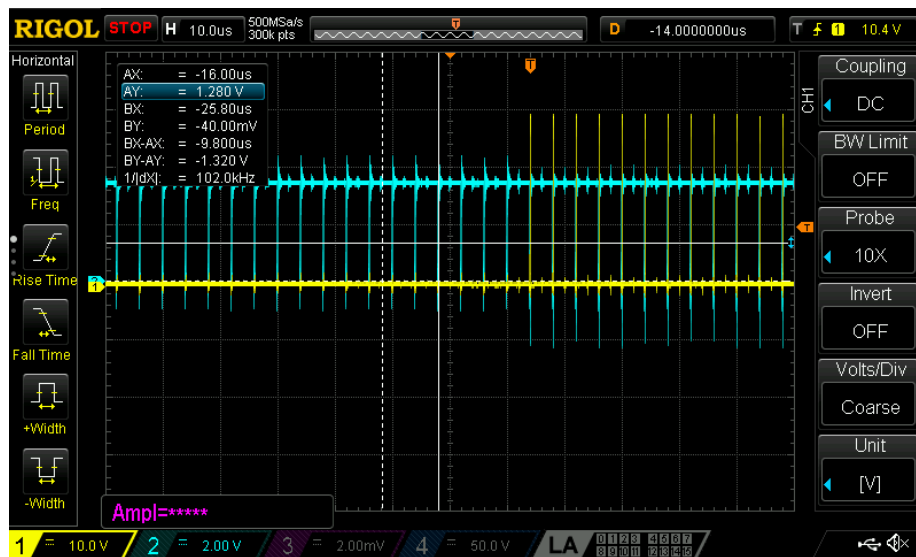
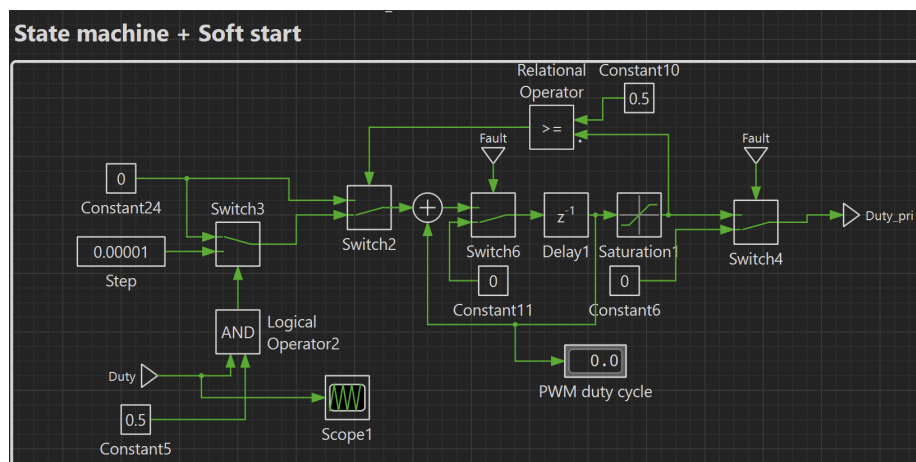


Figure 9 PWM signal (in blue) and V_{DS} of a primary low-side MOSFET (yellow) at converter start-up, showing the soft start sequence. (This was done by building the code and disabling the over-current protection that triggered directly after the code was flashed into the controller)

However, during our testing, we discovered that the soft start procedure was starting as soon as the PLECS code was “flashed” into the controller, and not when the input pow supply was actually turned on. For this reason, we modified the PLECS code to restart the soft start procedure every time we get out of a **fault state** (i.e. we turn on the power supply because an under voltage is detected if not the case). The following schematics represents the improved implementation :



/ 6 pt.

Q18: THERMAL MEASUREMENT AT THE NOMINAL OPERATING POINT

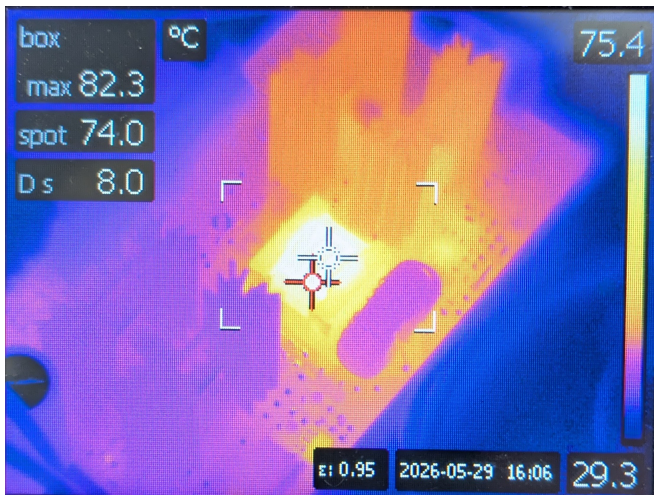
Before proceeding with the test of the full converter, it is important to ensure that it is not becoming excessively hot during operation. This is done by measuring the temperature at the nominal operating point. Connect the active load to the output connector (respecting the polarity) and set it to constant resistance mode (CR). The resistance should be sized according to your desired output voltage and a nominal power of 50 W. In the PLECS model, restore any changes previously made to bypass the protection. Set the fault threshold values to the appropriate values for your converter, keeping in mind the maximum values that can be read by your ADC. Ensure that the converter is run in open-loop by checking the state of the variable **PhiDebugEnabled**. In the same block, you will update the manual entry of phase shift until your desired output voltage is achieved, with V_{in} set to 50 V.

Let the converter run for 10 minutes. With the thermal camera, measure the temperature of the components on the PCB. Include the captured thermal image in your answer, identify the component(s) with the highest temperature(s) and explain why exactly this is the

case. Give an example of how the design could have been adapted to reduce the maximum measured temperature.

We conducted the test with a nominal input voltage of 50 V, a phase shift of 0.288 and a load of a value of:

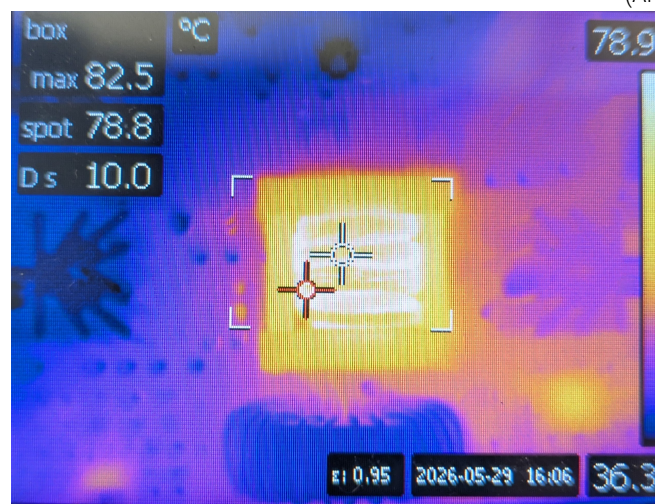
$$R_{load} = \frac{V_{out}^2}{P_{nom}} = \frac{24^2}{50} = 11.52\Omega$$



Picture 1: Thermal picture of the PCB after 10 minutes of test (Angle 1)



Picture 2: Thermal picture of the PCB after 10 minutes of test (Angle 2)



Picture 3: Thermal picture of the PCB after 10 minutes of test: Zoomed in at the transformer that represented the hot-spot of the board.

As seen in the three pictures above, the highest temperature reached was 82.5 °C, located at the transformer.

Why the transformer is the hottest component:

The transformer carries both the magnetizing current and the full transferred power at 250 kHz. At this switching frequency, core losses (hysteresis and eddy current losses) in the ferrite core are significant. In addition, the winding resistance causes copper losses proportional to I_{rms}^2 .

Both loss mechanisms are concentrated in a small volume, resulting in a high power density and therefore a high temperature rise. The transformer was intentionally designed to be compact (small core) to minimize weight, which reduces the surface area available for heat dissipation.

Design improvement to reduce maximum temperature:

The most effective improvement would be to use a larger core with a higher effective cross-sectional area. This would reduce the flux density, directly reducing core losses. Another possibility would be using a Litz wire winding instead of solid wire. This would reduce AC copper losses caused by the skin effect at 250 kHz, which are a significant contributor to winding losses at this frequency.

Remark:

We can also notice that the primary side heatsinks have a low temperature, which led us to remove them as mentioned before for the final design (As part of a weight optimization for our design).

Q19: OPEN-LOOP TEST

It is now time to test the full converter, using the theoretically calculated values of phase shift ϕ from Report 1 for the three values of input voltage considered. The set up and PLECS model remain the same as in the previous test. However, now you will update the manual entry of phase shift to the values that were previously calculated, and measure the resulting output voltage.

Use the oscilloscope to measure the input and output voltage at the test points. Record results for each of the previously calculated values of ϕ , including oscilloscope captures, and comment on the results.

The value of the load resistance for a $V_{out} = 24\text{ V}$ and $P_{nom} = 50\text{ W}$ is:

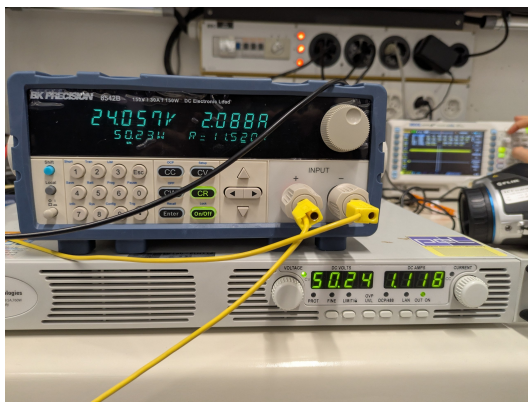
$$R_{load} = \frac{V_{out}^2}{P_{nom}} = \frac{24^2}{50} = 11.52\Omega$$

In report 1, we have computed the phase shift ϕ for each input voltage as follows:

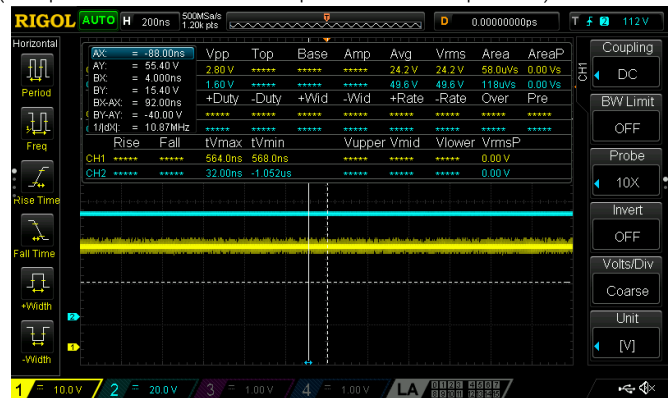
- $V_{min} = 30\text{ V} \Rightarrow \phi = 0.524\text{ rad}$ (or 2.618 rad)
- $V_{nom} = 50\text{ V} \Rightarrow \phi = 0.288\text{ rad}$ (or 2.853 rad)
- $V_{max} = 60\text{ V} \Rightarrow \phi = 0.236\text{ rad}$ (or 2.906 rad)

The tests were conducted with the computed phase values and we got the following results.

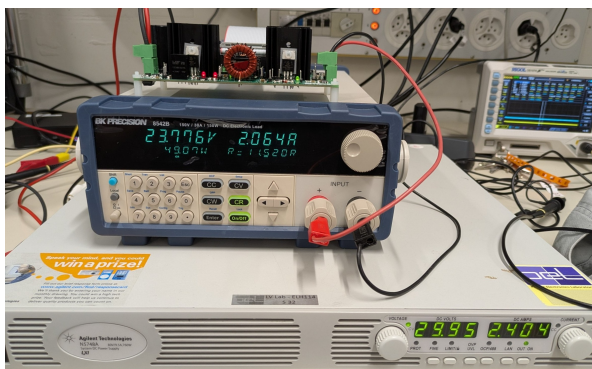
- For $V_{in} = 50\text{ V}$: The test with the computed phase of 0.288 rad gave the expected results with an output power and voltage of 50 W and 24 V respectively (See pictures 1 and 2 for setup and oscilloscope view)
- For $V_{in} = 30\text{ V}$: The tests with the computed phase of $\phi = 0.524\text{ rad}$ resulted in smaller output power and voltages (below the expected values). A tuning of the phase was performed and a phase of $\phi = 0.83\text{ rad}$ gave the expected results with an output power and voltage of 50 W and 24 V respectively (See pictures 3 and 4 for setup and oscilloscope view)
- For $V_{in} = 60\text{ V}$: The tests with the computed phase of $\phi = 0.236\text{ rad}$ resulted in smaller output power and voltages (below the expected values). Tuning of the phase was performed and a phase of $\phi = 0.16\text{ rad}$ gave the expected results with an output power and voltage of 50 W and 24 V respectively (See pictures 5 and 6 for setup and oscilloscope view)



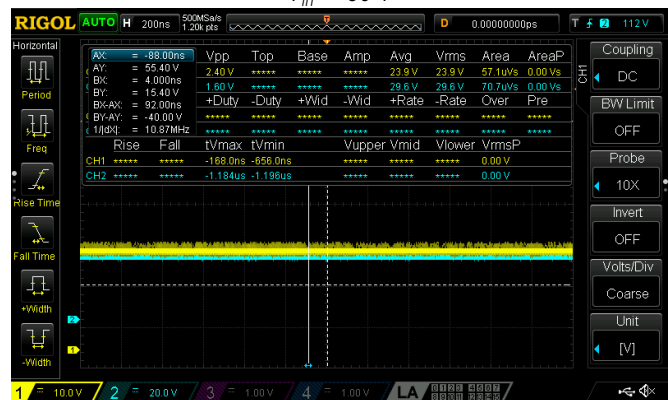
Picture 1: Setup for $V_{in} = 50\text{ V}$



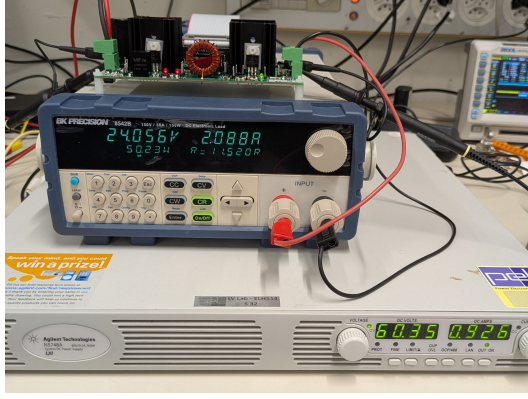
Picture 2: Oscilloscope view of V_{in} (Blue) and V_{out} (Yellow) for $V_{in} = 50\text{ V}$



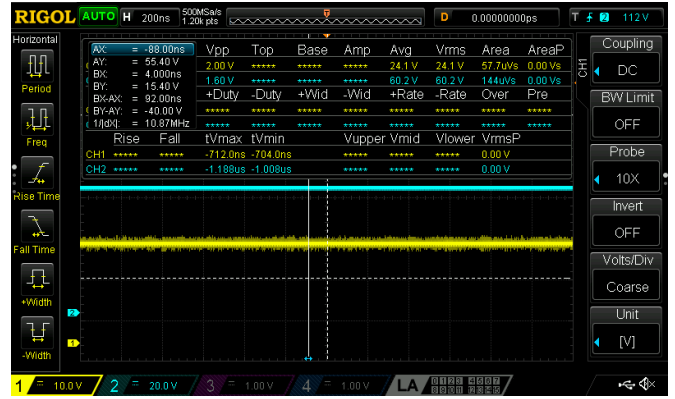
Picture 3: Setup for $V_{in} = 30\text{ V}$



Picture 4: Oscilloscope view of V_{in} (Blue) and V_{out} (Yellow) for $V_{in} = 30\text{ V}$



Picture 5: Setup for $V_{in} = 60V$

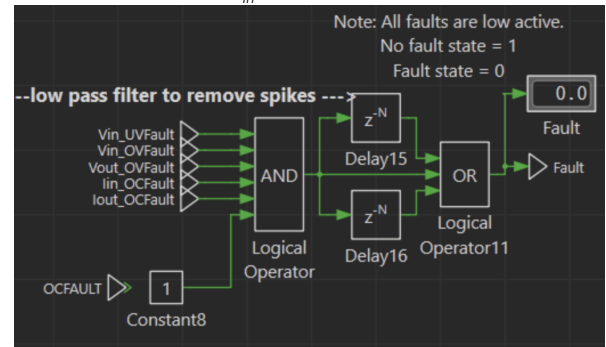


Picture 6: Oscilloscope view of V_{in} (Blue) and V_{out} (Yellow) for $V_{in} = 60V$

Remark:

As stated earlier, to conduct the tests, we had to disable the inductor over current fault, as this was often being triggered by some current spikes. For the other faults, we implemented a low pass filter to allow the operation of the controller despite the presence of eventual spikes. **Picture 7** shows the PLECS implementation of the low pass filter.

This low pass filter was initially used on all of the faults, but we ran into the limit of the program size (that can run on RAM only) of the DSP.



Picture 7: PLECS implementation of the Low pass filter on the faults

From the obtained measurements, we approximated the efficiencies using the current and voltage of the power supply and the load as follows :

$$\eta_{30V} = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} = \frac{23.78 \times 2.06}{29.95 \times 2.40} = \frac{48.9868}{71.88} = 0.681 = 68.1\%$$

$$\eta_{50V} = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} = \frac{24.06 \times 2.09}{50.24 \times 1.12} = \frac{50.2854}{56.2688} = 0.894 = 89.4\%$$

$$\eta_{60V} = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} = \frac{24.06 \times 2.09}{60.35 \times 0.93} = \frac{50.2854}{56.1255} = 0.896 = 89.6\%$$

We will compare these values to the closed loop efficiencies found later in the tests.

$$R_{load} = 11.52 \Omega$$

For minimum input voltage: $V_{out} = 23.78 V$

$I_{out} = 2.064 A$

$\varphi_{test} = 0.83 \text{ rad}$

For nominal input voltage: $V_{out} = 24.06 V$

$I_{out} = 2.088 A$

$\varphi_{test} = 0.288 \text{ rad}$

For maximum input voltage: $V_{out} = 24.06 V$

$I_{out} = 2.088 A$

$\varphi_{test} = 0.16 \text{ rad}$

/ 12 pt.

CLOSED-LOOP OPERATION

Q20: TESTING THE CLOSED-LOOP CONTROL

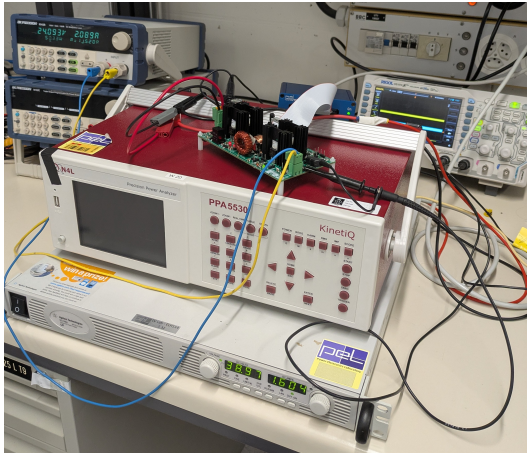
Enable closed-loop control by toggling the state of **PhiDebugEnabled**. Set the controller gains to those found during offline simulation. Use the active load in the same configuration as in the previous question. Step the input voltage from 60 V, eventually down to 30 V, and observe how the phase shift reference changes as a result of the closed-loop control. Include oscilloscope captures of input and output voltage as before, and comment on the results.

As computed before, the value of the load resistance for a $V_{out} = 24 V$ and $P_{nom} = 50 W$ is:

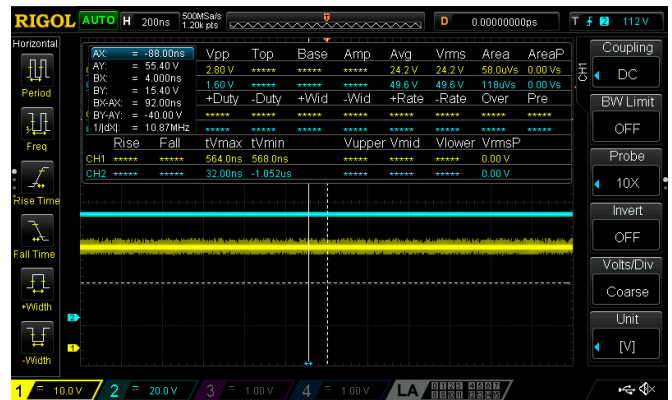
$$R_{load} = \frac{V_{out}^2}{P_{nom}} = \frac{24^2}{50} = 11.52\Omega$$

We conducted the closed loop tests using load put in resistive mode at 11.52Ω. The pictures below show the closed loop measurement setup as well as the results for 50 V, 30 V and 60 V of input voltages.

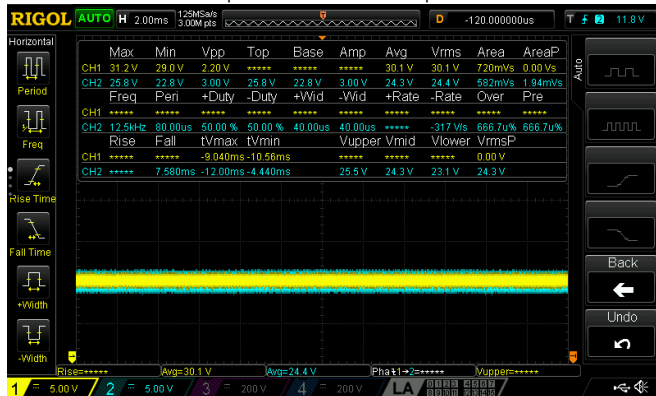
Remark: Because of the oscilloscope's probes inadequacies, some recorded values do not correspond exactly to the more exact ones recorded by the Electronic load (for e.g 24.4 V for the oscilloscope while the load showed 24.1 V)



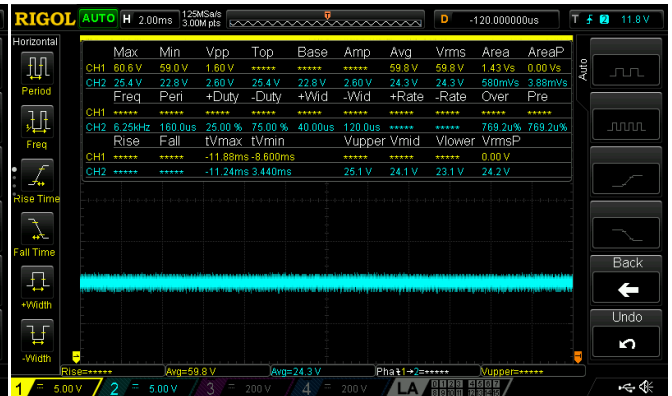
Picture 1: Setup for the closed loop measurements



Picture 2: Oscilloscope view of V_{in} (Blue) and V_{out} (Yellow) for $V_{in} = 50\text{ V}$



Picture 3: Oscilloscope view of V_{in} (Yellow) and V_{out} (Blue) for $V_{in} = 30\text{ V}$



Picture 4: Oscilloscope view of V_{in} (Yellow) and V_{out} (Blue) for $V_{in} = 60\text{ V}$

Results:

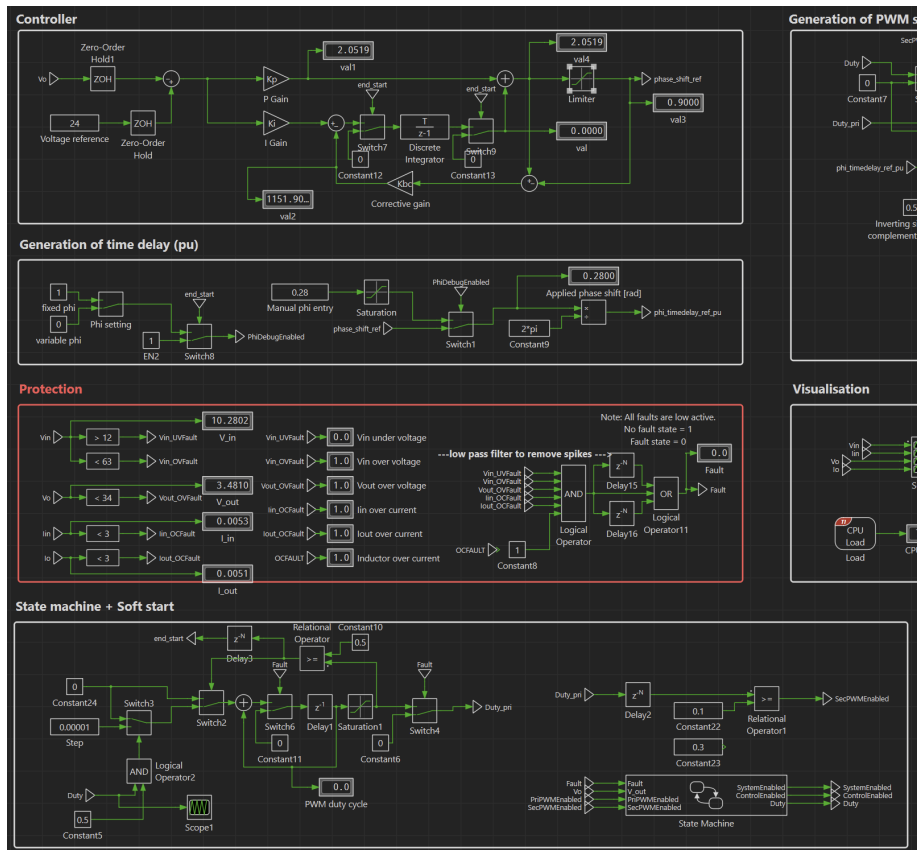
As seen in the pictures above, the voltage is regulated to the correct values. On the PLECS simulation, we also observed that the phase was changing with varying load and input voltage as it should.

Remark:

We had to reduce the values of the PI control because those were causing some oscillation (over correction of the voltage)

Addition:

we also implemented a system that start the closed loop operation only after the end of the soft start, so the controller does not register values during the start up and does not try to increase the phase to achieve the rated 24 V instantly. Picture 5 shows that implementation in PLECS.



Picture 5: Modified PLECS implementation for the closed loop start.

$$R_{load} = 11.52 \, \Omega$$

For maximum input voltage: $V_{out} = 24 \, \text{V}$

$$I_{out} = 2.06 \, \text{A}$$

$$\varphi_{ref} = 0.16 \, \text{rad}$$

For nominal input voltage: $V_{out} = 23.97 \, \text{V}$

$$I_{out} = 2.07 \, \text{A}$$

$$\varphi_{ref} = 0.286 \, \text{rad}$$

For minimum input voltage: $V_{out} = 24 \, \text{V}$

$$I_{out} = 2.1 \, \text{A}$$

$$\varphi_{ref} = 0.84 \, \text{rad}$$

/ 12 pt.

EFFICIENCY MEASUREMENTS

Once the correct operation of the converter has been verified, it is possible to evaluate its energetic performance.

Disable and turn off the primary side power supply and the secondary side active load. Connect the power analyzer in a way to measure the following variables:

- primary side voltage (from the input side positive terminal to the input side GND) - to be connected to the voltmeter terminals of Phase 2 of the power analyzer;
- primary side current (flowing from the power supply towards the converter) - to be connected to the ammeter terminals of Phase 2 of the power analyzer;
- secondary side voltage (from the output side positive terminal to the output side GND) - to be connected to the voltmeter terminals of Phase 1 of the power analyzer;
- secondary side current (flowing from the converter towards the active load) - to be connected to the ammeter terminals of Phase 1 of the power analyzer.

Turn on the power analyzer. Set the coupling to "dc" and add the measurement of the efficiency as "phase/next phase". Set the display in "three-phase mode". The converter output variables and the energetic efficiency can be read from the "Phase 1" column, while the converter input variables can be read from the "Phase 2" column of the display. Discard the reading displayed in the "Phase 3" column.

Q21: EFFICIENCY PLOT

Turn on the primary side power supply and the secondary side active load. The active load will be set to CR mode, and the resistance will be adapted based on the desired P_{out} for the test. Let the controller operate in closed-loop as before, to ensure that the output

voltage will be regulated to the desired level during the test. Fill in the table below with the efficiency measurements and the listed operating conditions. Then, include an efficiency plot of your results, and comment on the findings. Include pictures of the measurement set up.

In addition, suggest a way to modify the design in a way that reduces the losses and improves the efficiency of the converter.

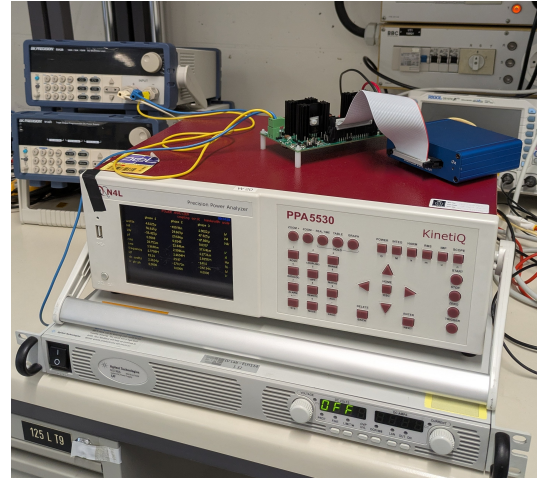
We start by calculating the required load resistance for each out-put power :

$$R_{load,50W} = \frac{V_{out}^2}{P_{out}} = \frac{24^2}{50} = 11.52\Omega$$

$$R_{load,40W} = \frac{V_{out}^2}{P_{out}} = \frac{24^2}{40} = 14.4\Omega$$

$$R_{load,30W} = \frac{V_{out}^2}{P_{out}} = \frac{24^2}{30} = 19.2\Omega$$

$$R_{load,20W} = \frac{V_{out}^2}{P_{out}} = \frac{24^2}{20} = 28.8\Omega$$



Picture 1: Setup for the closed loop measurements. it includes : Power supply, electronic load (in constant R mode) and power meter

The results of the tests are shown in the pictures below, with input being phase 2 and output phase 3:

POWER ANALYZER 00:23:49				
coupling ac+dc bandwidth wide				
	phase 1	phase 2	phase 3	
watts	4.2886μ	-31.838	-19.720	W
VA	53.829μ	31.859	19.721	VA
WAr	53.658μ	-1.1545	-239.02m	WAr
pf	0.0797	0.9993	0.9999	
rms	28.408m	30.405	23.879	V
rms	1.8948m	1.0583	825.87m	A
frequency	1.7701M	0.0000	0.0000	Hz
HZ	11.50	0.000	0.000	%
dc watts	50.908n	-31.838	-19.720	W
V ph-ph	0.0000	0.0000	0.0000	V

$$\eta(20\text{ W}, 30\text{ V}) = \frac{19.72}{31.84} = 61.93\%$$

POWER ANALYZER 00:23:11				
coupling ac+dc bandwidth wide				
	phase 1	phase 2	phase 3	
watts	2.3172μ	-22.191	-19.781	W
VA	54.505μ	22.254	19.782	VA
WAr	54.456μ	-1.6746	-223.17m	WAr
pf	0.0425	0.9972	0.9999	
rms	28.427m	50.080	23.905	V
rms	1.9174m	444.37m	827.53m	A
frequency	1.7706M	0.0000	0.0000	Hz
HZ	34.68	0.000	0.000	%
dc watts	664.47n	-22.191	-19.781	W
V ph-ph	0.0000	0.0000	0.0000	V

$$\eta(20\text{ W}, 50\text{ V}) = \frac{19.78}{22.25} = 88.90\%$$

POWER ANALYZER 00:23:28				
coupling ac+dc bandwidth wide				
	phase 1	phase 2	phase 3	
watts	2.0193μ	-24.194	-19.812	W
VA	54.139μ	24.230	19.816	VA
WAr	-54.101μ	-2.1552	-269.67m	WAr
pf	0.0373	0.9861	0.9998	
rms	28.347m	60.060	23.927	V
rms	1.9099m	404.43m	828.16m	A
frequency	1.7705M	0.0000	5.9563	Hz
HZ	156.2	0.000	0.000	%
dc watts	318.94n	-24.194	-19.812	W
V ph-ph	0.0000	0.0000	0.0000	V

$$\eta(20\text{ W}, 60\text{ V}) = \frac{19.82}{24.30} = 81.56\%$$

POWER ANALYZER 00:23:46				
coupling ac+dc bandwidth wide				
	phase 1	phase 2	phase 3	
watts	893.83n	-44.158	-29.879	W
VA	56.038μ	44.170	29.880	VA
WAr	56.031μ	-1.0445	-242.31m	WAr
pf	0.0160	0.9997	1.0000	
rms	28.581m	30.259	23.998	V
rms	1.9607m	1.4597	1.2451	A
frequency	1.7706M	0.0000	0.0000	Hz
HZ	11.59	0.000	0.000	%
dc watts	1.7604μ	-44.158	-29.879	W
V ph-ph	0.0000	0.0000	0.0000	V

$$\eta(30\text{ W}, 30\text{ V}) = \frac{29.88}{44.17} = 67.65\%$$

POWER ANALYZER 00:24:21				
coupling ac+dc bandwidth wide				
	phase 1	phase 2	phase 3	
watts	1.6267μ	-32.834	-29.826	W
VA	56.365μ	32.876	29.826	VA
WAr	56.341μ	-1.6501	-228.31m	WAr
pf	0.0289	0.9987	1.0000	
rms	28.645m	50.302	23.975	V
rms	1.9677m	653.57m	1.2441	A
frequency	1.7707M	0.0000	0.0000	Hz
HZ	-168.6	0.000	0.000	%
dc watts	2.3035μ	-32.834	-29.826	W
V ph-ph	0.0000	0.0000	0.0000	V

$$\eta(30\text{ W}, 50\text{ V}) = \frac{29.83}{32.88} = 90.72\%$$

POWER ANALYZER 00:23:59				
coupling ac+dc bandwidth wide				
	phase 1	phase 2	phase 3	
watts	2.7016μ	-34.417	-29.752	W
VA	53.933μ	34.482	29.754	VA
WAr	-53.865μ	-2.1200	-358.53m	WAr
pf	0.0501	0.9981	0.9999	
rms	28.456m	60.317	23.940	V
rms	1.8953m	571.68m	1.2428	A
frequency	1.7698M	0.0000	3.1608	Hz
HZ	22.95	0.000	0.000	%
dc watts	429.13n	-34.417	-29.752	W
V ph-ph	0.0000	0.0000	0.0000	V

$$\eta(30\text{ W}, 60\text{ V}) = \frac{29.75}{34.48} = 86.28\%$$

POWER ANALYZER 00:25:09				
coupling ac+dc bandwidth wide				
	phase 1	phase 2	phase 3	
watts	-1.7161μ	-57.604	-39.961	W
VA	54.338μ	57.615	39.962	VA
WAr	54.311μ	-1.1465	-275.99m	WAr
pf	0.0316	0.9998	1.0000	
rms	28.456m	30.205	24.031	V
rms	1.9095m	1.9075	1.6629	A
frequency	1.7702M	0.0000	0.0000	Hz
HZ	0.005	0.000	0.000	%
dc watts	628.23n	-57.604	-39.961	W
V ph-ph	0.0000	0.0000	0.0000	V

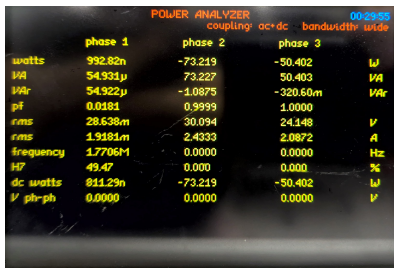
$$\eta(40\text{ W}, 30\text{ V}) = \frac{39.96}{57.62} = 69.36\%$$

POWER ANALYZER 00:25:24				
coupling ac+dc bandwidth wide				
	phase 1	phase 2	phase 3	
watts	-2.1809μ	-44.178	-40.049	W
VA	54.625μ	44.202	40.049	VA
WAr	-54.581μ	-1.4574	-188.80m	WAr
pf	0.0399	0.9995	1.0000	
rms	28.375m	50.207	24.057	V
rms	1.9251m	880.41m	1.6648	A
frequency	1.7703M	0.0000	0.0000	Hz
HZ	67.13	0.000	0.000	%
dc watts	535.39n	-44.178	-40.049	W
V ph-ph	0.0000	0.0000	0.0000	V

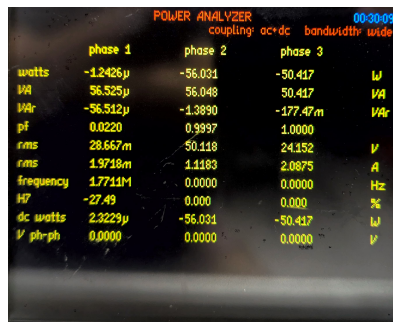
$$\eta(40\text{ W}, 50\text{ V}) = \frac{40.05}{44.20} = 90.61\%$$

POWER ANALYZER 00:25:04				
coupling ac+dc bandwidth wide				
	phase 1	phase 2	phase 3	
watts	-4.3606μ	-45.017	-40.072	W
VA	56.96μ	45.052	40.073	VA
WAr	56.528μ	-1.7651	-287.26m	WAr
pf	0.0769	0.9992	1.0000	
rms	23.078m	60.136	24.061	V
rms	1.9498m	748.41m	1.6655	A
frequency	1.7725M	0.0000	0.0000	Hz
HZ	-14.49	0.000	0.000	%
dc watts	2.7944μ	-45.017	-40.072	W
V ph-ph	0.0000	0.0000	0.0000	V

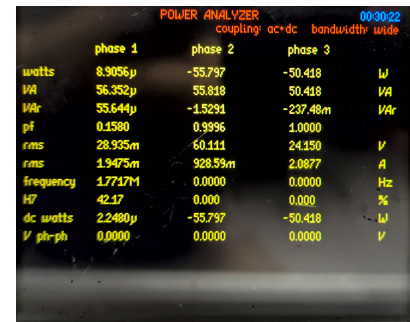
$$\eta(40\text{ W}, 60\text{ V}) = \frac{40.07}{45.05} = 88.95\%$$



$$\eta(50 \text{ W}, 30 \text{ V}) = \frac{50.40}{73.23} = 68.83\%$$



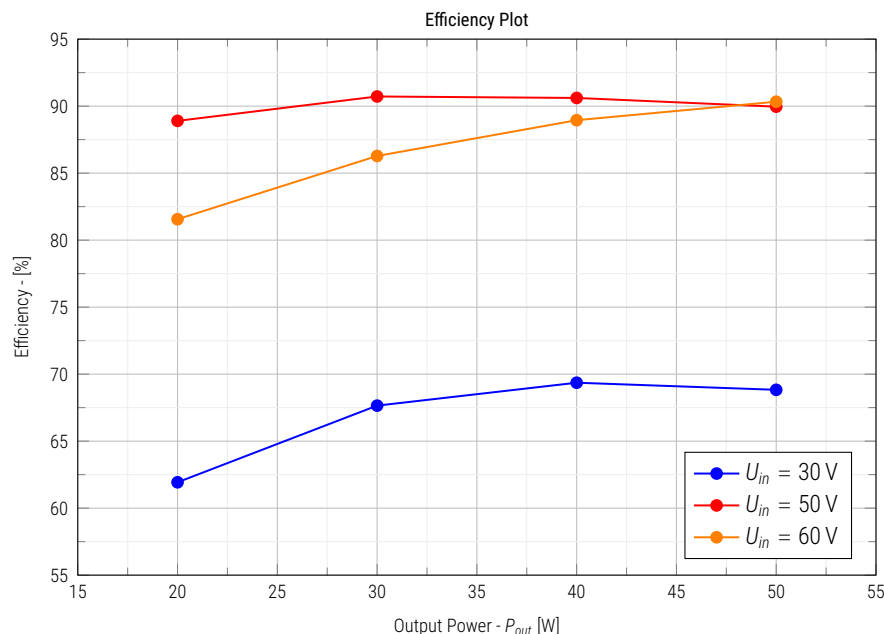
$$\eta(50 \text{ W}, 50 \text{ V}) = \frac{50.42}{56.05} = 89.96\%$$



$$\eta(50 \text{ W}, 60 \text{ V}) = \frac{50.42}{55.82} = 90.33\%$$

Table 2 Efficiency Measurements.

$U_{in} (\downarrow)$	$P_{out} (\rightarrow)$	20 W	30 W	40 W	50 W
30 V		61.93%	67.65%	69.36%	68.83%
50 V		88.90%	90.72%	90.61%	89.96%
60 V		81.56%	86.28%	88.95%	90.33%



Results:

We find an efficiency above 90% with some operating conditions, which we are quite happy with.

Observations:

The closed loop values are quite close from the values we found in open loop in Q19, which show that closed loop is not reducing the efficiency of the converter.

We find that the efficiency values are lower than the one calculated in report 2, especially the worst case value at 30V, which was calculated to 86% but turned out to be a bit less than 70%.

We also observe that the efficiency is lower for the lower output power. This can be explained by the fact that the ICs, LEDs, voltage converter are consuming a constant amount of power. This amount is obviously bigger in proportion when the output power lowers, thus reducing efficiency.

Suggested improvement:

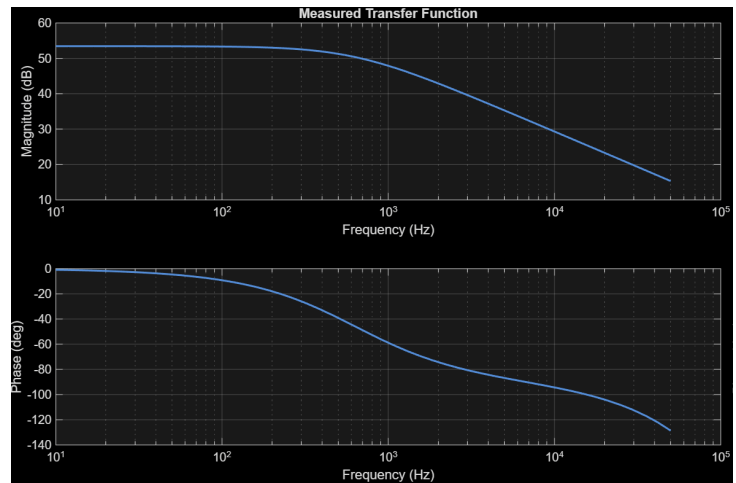
By looking at what is getting the hotter, that is the transformer, we know that this is where most of the losses occur. We believe that building a larger transformer with larger wires and core might help with efficiency. But, as we choose to aim for the lightest design, we have a really small transformer.

ADDITIONAL SECTION

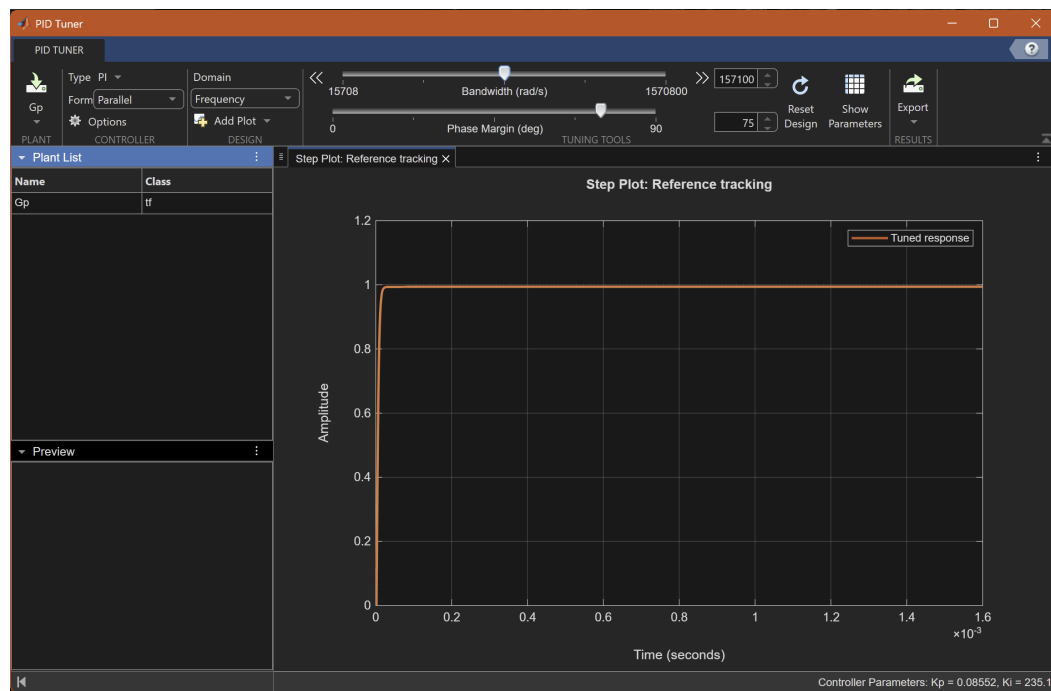
We further empirically tuned the PI values of our controller to have a better behavior. We ended with values of $K_p = 0.1$ and $K_i = 100$. In order to verify those value, we used a PLECS simulation to mesure the frequency response of the converter. Then we used Matlab to estimate the transfer function from the frequency response. Finally, we input that into matlab control tuner to get an estimate of the PI values. The obtained values were $K_p = 0.0856$ and $K_i = 235$, which were indeed quite close from our experimental values !

$$G_p = \frac{-1.761e06 s + 1.636e12}{s^2 + 8.934e05 s + 3.482e09}$$

Estimated transfert function from the measured one



Measured transfer function



Results from Matlab control tuner