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Title

R3: DAB CONVERTER — SCHEMATIC AND PCB DESIGN

Course Name
EE-365 Power Electronics

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OVERVIEW

In this third part, the project addresses the schematic and PCB design of the Dual Active Bridge (DAB) converter according to the specifications assigned to your group. **Fill out Table 1** with the parameters assigned to your group. In this report, you will complete the selection of all necessary components and populate the provided schematic and PCB layout using Altium Designer. The concept of the complete schematic of the DAB converter is illustrated in Fig. 1.

The list of available SMD capacitors, SMD resistors, that can be used for your design is provided in the Appendix section. The use of components not listed in the Appendix is allowed **if and only if** authorized by a TA or explicitly stated in the instructions in this report.

To provide your answers and explanations, use the framed boxes below each question. **In case multiple units are employed to realize the same circuit component, append additional frame boxes in the answers, and add numbers to the corresponding designators (e.g., in case of multiple parallel input capacitors, denote them as $C_{in,1}$, $C_{in,2}$, etc...).** Please note a maximum limit of **four components** in series or parallel when targeting a specific design value.

A project template for Altium Designer will be provided. It should be noted that the schematic sheet has been divided into several blocks; according to the block name, you are asked to complete the placement of the components. All the used components have been included in the datasheet. Consider what follows before proceeding further:

- Before proceeding with the report, according to Fig. 1, populate the power-stage part of the schematic diagram with the components in the bottom of the schematic. For the semiconductor devices, add the part number of the selected devices in the comment of the device model.
- While proceeding from **Q1 to Q40**, the values of passive components should be put in the comment as well.
- While proceeding from **Q1 to Q40**, it is suggested to populate the schematic diagram step-by-step.

By following the steps outlined in this report, you will be able to prepare and manufacture the Dual Active Bridge (DAB) converter PCB. Note that you may need to create custom footprints for certain components. When doing so, carefully consult the component datasheets; as a general rule, ensure the pad hole diameter is 1.2 times the diameter of the component lead pins.

Note: Installation guideline of the Alitum Designer can be found in **LINK**.

Table 1 Given parameters and design requirements for the DAB converter.

Property	Value	Unit
$P_{out,nom}$	50	W
$V_{in,nom}$	50	V
$V_{in,min}$	30	V
$V_{in,max}$	60	V
V_{out}	24	V
$\Delta V_{out,pp,rel}$	2	%
f_{sw}	250	kHz
$V_{aux,out}$	18	V
$P_{aux,out}$	5	W

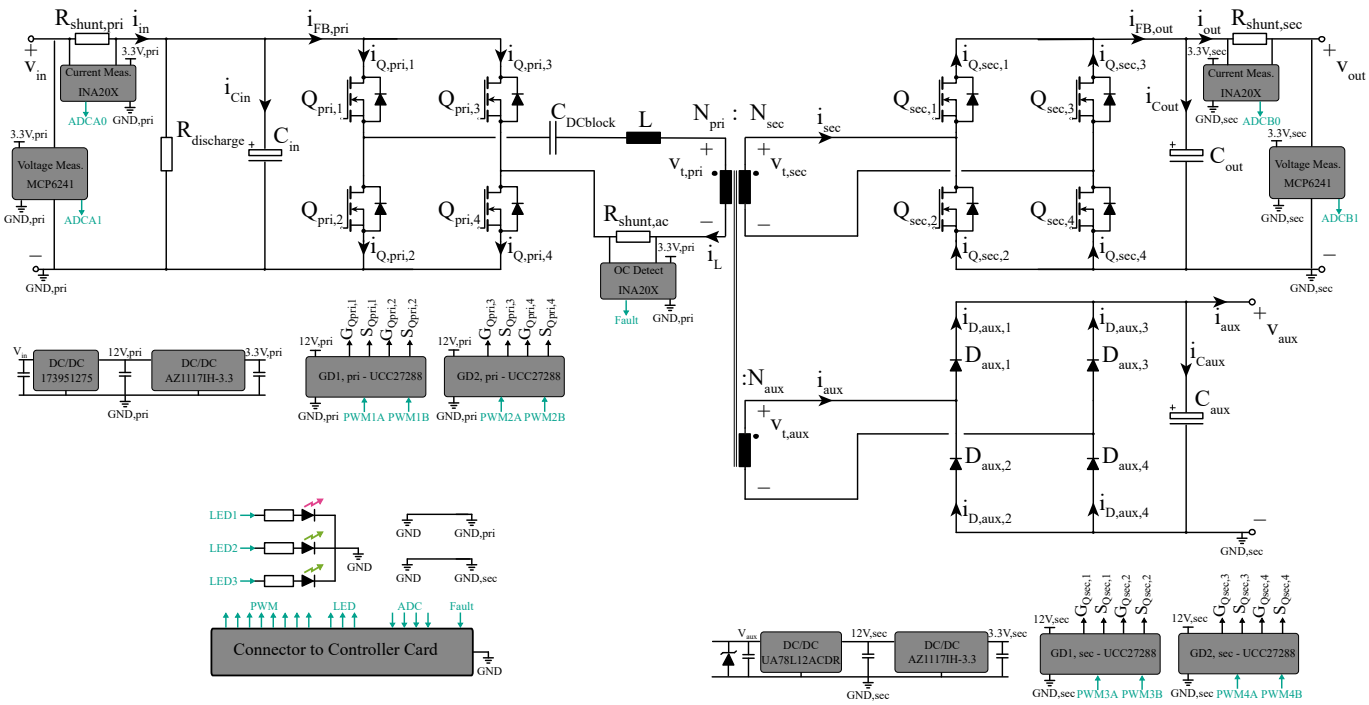


Figure 1 Circuit diagram of the DAB converter.

POWER STAGE

Q1: SELECTION OF THE INPUT ELECTROLYTIC CAPACITORS

According to the calculation in Report 1, select an input electrolytic capacitor from below list (Table 2).

Table 2 Aluminum electrolytic capacitors

Part number	Capacitance	Rated Voltage DC
39D507G030FL6	500 uF	30 VDC
MAL215236109E3	10 uF	400 VDC
UHW2A681MHD	680 uF	100 VDC

Selected input electrolytic capacitor: UHW2A681MHD | C_{in}=680 10^{-6}F | $V_{rated\text{-}C,in}$=100 V | / 1 pt.

Q2: SELECTION OF THE INPUT CERAMIC CAPACITOR

Aluminum electrolytic capacitors exhibit inductive behavior at high frequencies (typically above 10 kHz) due to their Equivalent Series Inductance (ESL). This characteristic significantly diminishes their effectiveness in filtering high-frequency voltage ripples. Consequently, ceramic capacitors are commonly connected in parallel to compensate for this limitation.
The muRata GRM31CZ72A475KE11L and TDK C5750X7S2A226M280KB have been specified as potential input ceramic capacitors. However, it is crucial to account for the DC bias effect, as the effective capacitance of most ceramic capacitors drops substantially under applied voltage. Based on the requirements established in Report 1, please calculate the necessary number of parallel capacitors after verifying the capacitance-voltage characteristics in the respective datasheet.
Note: The TDK C5750X7S2A226M280KB uses a 2220 package. Since its price is eight times that of the muRata GRM31CZ72A475KE11L, please prioritize the use of the muRata component for the input capacitor bank.

$C_{in,ceramic,min}$: 1.62 10^{-6} F | Input capacitor part number: GRM31CZ72A475KE1

$C_{selected,@60Vdc}$= 1.88 10^{-6} F | Number of parallel capacitor: 2 | / 2 pt.

Q3: SELECTION OF THE INPUT DISCHARGE RESISTOR

According to the calculation in Report 1, select the input discharge resistor.

Selected input discharge resistor: 28.7 kΩ (KIT-RMCF1206FT-05) | Package for input discharge resistor: 1206/3216 | / 1 pt.

Q4: SELECTION OF THE DC BLOCKING CAPACITOR

The muRata GRM31CZ72A475KE11L or TDK C5750X7S2A226M280KB has been specified for use as the DC-blocking capacitor. It is critical to account for the power dissipation across these components. Please consult the datasheet to determine the Equivalent Series Resistance (ESR) at your specific operating frequency. Based on this value, estimate the power loss per capacitor (assuming a parallel configuration if multiple units are used).

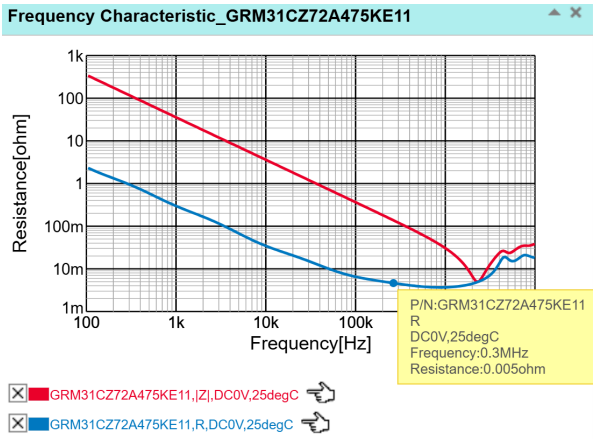
From report 1, $C_{DCBlock,min} = 4.86 \times 10^{-6} F$.

We choose the GRM31CZ72A475KE11 capacitor. Two capacitors are required because a single $4.7\mu F$ unit is below the minimum $C_{DCblock,min} = 4.86\mu$F.
Two in parallel give $9.4\mu F > 4.86\mu F$

From **murata website** we get the ESR graph and find the following:

$$ESR \approx 5\,m\Omega \text{ at } 250 \text{ kHz}$$

The DC blocking capacitor is in series with the primary winding and therefore carries the full primary inductor current $I_{pri,rms} = 2.08$. With 2 capacitors in parallel, this current divides equally leading to:



$$P_{loss/cap} = \left(\frac{I_{pri,rms}}{2}\right)^2 \times ESR = (1.04)^2 \times 5 \times 10^{-3} = 5.408 \text{ mW} << 80 \text{ mW}$$

So the power dissipation is smaller than the limit value defined in Table 4

Capacitor part number: GRM31CZ72A475KE1	ESR: 5×10^{-3} Ω @ 250 KHz	
Number of parallel capacitor: 2	Loss per capacitor: 5.41×10^{-3} W	/ 2 pt.

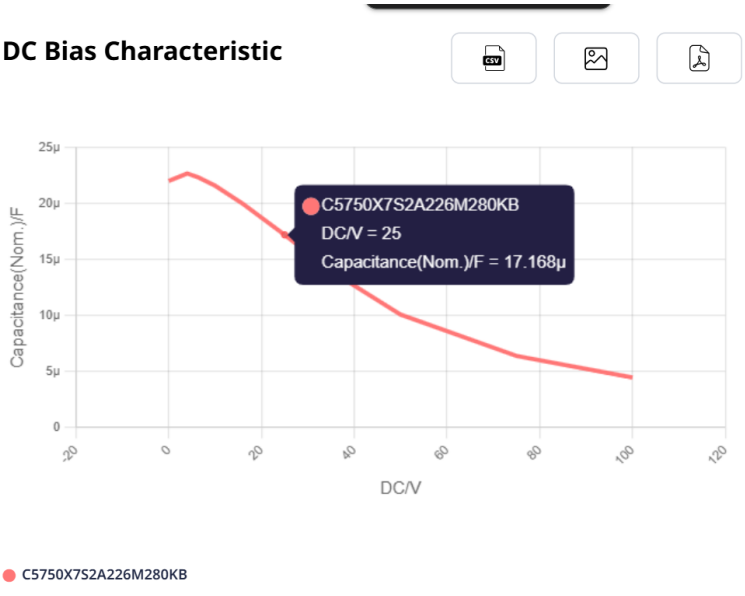
Q5: SELECTION OF THE OUTPUT CAPACITOR

According to the calculation in Report 1, select the output capacitor from the available SMD capacitor (see Appendix). Again, you need check the datasheet to get the capacitance at DC-bias voltage.
Note: It is not necessary to match the calculated value exactly, as long as the selection of the capacitance higher than the calculated value, the selection should be good. Try to use fewer capacitor here.

From report 1, we found $C_{out} = 6.12 \times 10^{-6}$ F.
We choose the TDK-C5750X7S2A226M280KB capacitor.

From **TDK page** we get the DC Bias Characteristic graph, we get the value of the capacitance at $V_{out} = 24$ V:

$$C_{selected,@Vout} \approx 17.2 \times 10^{-6} \text{ F} > 6.12 \times 10^{-6} \text{ F}$$



Selected output capacitor: 5750X7S2A226M280KB (TDK)	Number of parallel capacitor: 1	
$C_{selected,@Vout}$ = 17.2 µF	$V_{rated-C,out}$ = 100 V	/ 2 pt.

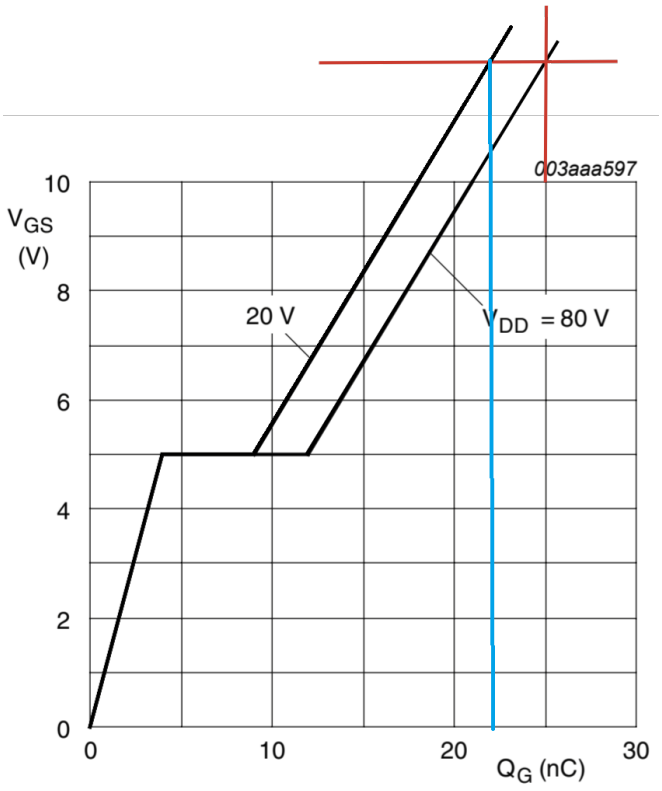
Q6: EXTRACT THE GATE CHARGE (Q_G) FOR SELECTED MOSFETS

Indicate the part number of the MOSFETs you selected in report 1. Then, check their datasheets, specifically, the graph of "Typical Gate Charge vs.Gate-to-Source Voltage". Extract and provide the gate charge Q_g for both primary and secondary devices when the gate-drive voltage is at 12 V, and indicate how you extracted them in the framed box.

Our MOSFET type is the Nexperia PHP18NQ11T(Type 6) for both the primary and the secondary side.

As the plot was too small, we had to extend it. As the primary input voltage can go up to 60V, we look at the 80v curve. $Q_{g,pri}$ for a V_{GS} value of 12v is around 25nC.

For the secondary side, the voltage should not exceed 24V, so we take the 20v curve as an estimate. We get that $Q_{g,sec}$ for a V_{GS} value of 12v is around 23nC.



$$I_D = 3A; V_{DD} = 20V \text{ and } 80V$$

Figure 2 Gate charge vs. gate-to-source voltage of primary and secondary MOSFET.

MOSFET, pri.: no 6 (PHP18NQ11T)	$Q_{g,pri}$ = 25 nC	MOSFET, sec.: no 6 (PHP18NQ11T)	$Q_{g,sec}$ = 23 nC	/ 1 pt.

Q7: EXTRACT THE INTERNAL GATE RESISTANCE ($R_{G,INT}$) FOR SELECTED MOSFETS

Check the datasheets of the selected MOSFETs, then extract the internal gate resistance $R_{g,int}$. Only in case the value is not provided by the manufacturer, you can assume a value of 2Ω.

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$R_{g,int,pri}$ = 2 Ω	$R_{g,int,sec}$ = 2 Ω	/ 1 pt.

GATE DRIVER ON THE PRIMARY SIDE

There are two typical solutions to drive a half-bridge:
1. Using two single-channel gate drivers to drive two devices independently;
2. Using a dual-channel gate driver based on bootstrap technology.

The first solution provides more flexibility but usually needs an extra isolated DC power supply. In this course, a dual-channel gate driver is used. The typical circuit diagram of a half-bridge gate driver and half-bridge MOSFET is shown in Fig. 3.

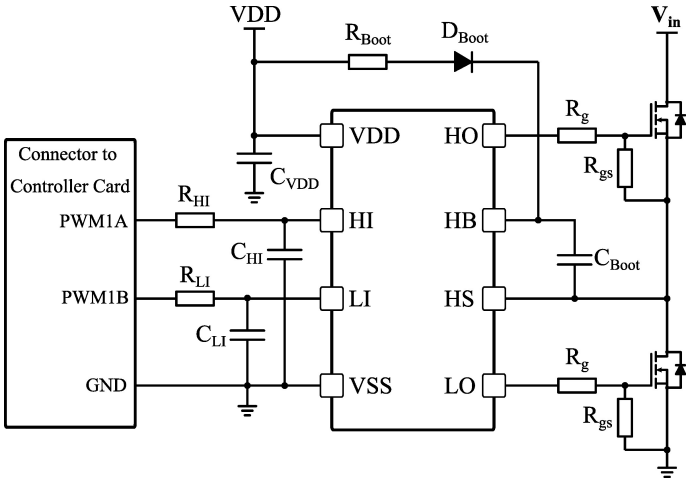


Figure 3 Typical application schematic of a dual-channel gate driver with bootstrap technique.

In this project, we ask you to use the half-bridge gate driver UCC27288 from Texas Instruments. Its surrounding components should be calculated and selected according to your choice of MOSFETs. In this section, follow questions Q8 to Q15 to design the primary side gate driver circuit.

Note: The datasheet of the UCC27288 provides a detailed design procedure. Read it carefully at this **LINK**. In this project, the gate driving voltage is set as 12V.

Q8: CALCULATION OF THE BOOTSTRAP CAPACITOR

Refer to section 8.2.2.1 of the UCC27288 datasheet, and calculate the capacitance of the bootstrap capacitor following the step-by-step procedure. Report calculation procedure in the framed box, and calculated values in the answer boxes. Then, choose the closest standard capacitance value (see the Appendix), and report selected capacitor and its voltage rating in the answer boxes.
Note: In this calculation, you can consider the forward voltage drop over the diode D_{Boot} to be 0.9 V;

From section 8.2.2.1, we get the following formula:

$$\Delta V_{HB} = V_{DD} - V_{DH} - (V_{HBR(max)} - V_{HBHys}) = 12 - 0.9 - (7.1 - 0.5) = 4.5\text{V}$$

$$Q_{TOTAL} = Q_G + I_{HBS,max} \times \left(\frac{D_{MAX}}{f_{SW}}\right) + \left(\frac{I_{HB}}{f_{SW}}\right) = 25 \times 10^{-9} + 50 \times 10^{-6} \times \left(\frac{0.5}{250 \times 10^3}\right) + \left(\frac{0.4 \times 10^{-3}}{250 \times 10^3}\right) = 26.7 \times 10^{-9}\ \text{C}$$

$$C_{BOOT,min} = \frac{Q_{TOTAL}}{\Delta V_{HB}} = \frac{26.7 \times 10^{-9}}{4.5} = 5.93\ \text{nF}$$

We need to select a value of bootstrap capacitor greater than $C_{\text{boot,min}}$.
From the datasheet: *"The bootstrap and bias capacitors must be ceramic types with X7R dielectric or better. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to"*, that is 12 · 2 = 24V. We will select the **C1206C683J1RECAUTO** capacitor that has $(C_{\text{boot,selected}}, V_{\text{Cboot,rated}}) = (68\,nF, 100V)$. This respects the margin for both the capacitor value and the rated voltage. It also uses a X7R which is what was recommended by the datasheet.

ΔV_{HB} = 4.5 V | $Q_{TOTAL} = 26.7 \times 10^{-9} C$ | $C_{boot,min}$ = 5.93 10^{-9}F

$C_{boot,selected}$ = 68 10^{-9}F | $V_{Cboot,rated}$ = 100 V / 3 pt.

Q9: SELECTION OF THE VDD CAPACITOR

Refer to section 8.2.2.1 of the UCC27288 datasheet, and calculate the required VDD capacitor. Then, choose the closest standard capacitance value (see the Appendix). Report selected capacitor and its voltage rating in the answer boxes.

From the datasheet, we are adviced to use a VDD capacitor of a value 10 times higher that the Bootstrap capacitor.

$$C_{VDD,selected} = 10 \times C_{boot,selected} = 10 \times 68nF = 0.68\mu F$$

The rated voltage must be twice the maximum voltage, that is $2 \times VDD = 24$V, and have a dielectric of type X7R. We choose to use the **C1206C105K3RACTU** capacitor as it satisfies all of the above. Its capacitance ration is 1 μF.

$C_{VDD,selected}$ = 1 μF | $V_{CVDD,rated}$ = 25 V / 2 pt.

Q10: SELECTION OF THE BOOTSTRAP SERIES RESISTOR

The series resistance R_{boot} will limit the peak current at the bootstrap diode during start-up, but it should also be carefully selected as it introduces a time constant with the bootstrap capacitor given by

$$\tau = R_{boot} C_{boot}. \tag{1}$$

This time constant is related to the start-up time, which influences the load dv/dt. In this project, the selected R_{boot} should satisfy

$$3R_{boot} C_{boot} < 10 D_{min} / f_{sw}. \tag{2}$$

where D_{min} is the minimal duty cycle of the low-side device during the soft start. In this project course, D_{min} is set as 0.05. This will ensure that the capacitor can be charged sufficiently at the minimum duty cycle in 10 switching periods.
Additionally, the bootstrap resistor chosen must be able to withstand high power dissipation during the first charging sequence of the bootstrap capacitor. This energy and average power can be estimated by

$$E_{boot} = \frac{1}{2} C_{boot} V_{boot}^2, \quad P_{R(boot)} = E_{boot} \cdot f_{sw} \tag{3}$$

In this specific project course, we suggest that R_{boot} be in the range of 1 Ω to 10 Ω. Choose a proper package for this resistor.

R_{boot} = 4.99 Ω | $P_{R(boot)}$ = 1.05 W / 2 pt.

Q11: CALCULATE THE VOLTAGE STRESS AND PEAK CURRENT OVER THE BOOTSTRAP DIODE

When the high-side device is on, the bootstrap diode will be reverse-biased. The selection of the bootstrap diode should consider the voltage stress when the diode is reverse-biased and the peak current through the diode during the start-up charging.

In this project course, the diode ES2C will be used as the bootstrap diode.

$V_{Dboot,peak}$ = 59.1 V | $I_{Dboot,peak}$ = 2.22 A / 1 pt.

Q12: SELECTION OF THE EXTERNAL GATE RESISTOR

In gate drivers for high-frequency converters, parasitic inductance and parasitic capacitance can cause voltage and current oscillations on the gate of the power MOSFETs. These oscillations can cause the breakdown of the device and disturb adjacent circuits. External gate resistors are typically used to slow down the turn-on and turn-off of the devices, thus mitigating these oscillations. Refer to Section 8.2.2.4, select the external gate resistor, and calculate the source and sink current of the gate driver (the symbols are indicated in the datasheet). In this project course, we suggest that the external gate resistor is in the range of 5 Ω to 10 Ω.

Note: In the practical experimental test, you should capture the waveform of the gate-source voltage. If there are obvious oscillations that may result in fault switching on, i.e., the amplitude of the oscillations is higher than the turn-on threshold, the resistor should be increased.

We choose the gate resistor $R_{GATE} = R_g = 10\,\Omega$, which is the only available individual resistor within the required 5–10 Ω range (RMCF1206FT10R0).
From the previous questions: $V_{DD} = 12\,V$, $V_{DH} = 0.9\,V$, $R_{GFET(int)} = 2\,\Omega$.
The internal gate driver resistances are computed from the **UCC27288** datasheet (as defined in the Q14 note):

$$R_{HOH} = V_{HOH}/I_{HO} = 0.42\,V/100\,mA = 4.2\,\Omega$$

$$R_{HOL} = V_{HOL}/I_{HO} = 0.40\,V/100\,mA = 4.0\,\Omega$$

$$R_{LOH} = V_{LOH}/I_{LO} = 0.42\,V/100\,mA = 4.2\,\Omega$$

$$R_{LOL} = V_{LOL}/I_{LO} = 0.40\,V/100\,mA = 4.0\,\Omega$$

Using Equations 9–12 from Section 8.2.2.4 of the datasheet:

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{GATE} + R_{GFET(int)}} = \frac{12 - 0.9}{4.2 + 10 + 2} = \frac{11.1}{16.2} = 0.685\,A$$

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{GATE} + R_{GFET(int)}} = \frac{11.1}{4.0 + 10 + 2} = \frac{11.1}{16.0} = 0.694\,A$$

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{GATE} + R_{GFET(int)}} = \frac{12}{4.2 + 10 + 2} = \frac{12}{16.2} = 0.741\,A$$

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{GATE} + R_{GFET(int)}} = \frac{12}{4.0 + 10 + 2} = \frac{12}{16.0} = 0.750\,A$$

All currents are below the ±3 A peak rating of the UCC27288.

R_g = 10 Ω	I_{OHH} = 0.685 A	I_{OLH} = 0.694 A	I_{OHL} = 0.741 A	I_{OLL} = 0.75 A	/ 2 pt.

Q13: SELECTION OF THE EXTERNAL GATE-SOURCE RESISTOR

The gate-source resistor (often called a pull-down resistor for N-channel devices) is a crucial safety component in MOSFET circuits. It prevents the MOSFET from turning on accidentally when the control signal is disconnected or undefined.
For most power electronics applications (e.g., motor drives, DC-DC converters), the standard value lies between 5 kΩ and 15 kΩ.

R_{gs} = 10 kΩ	P_{Rgs} = 14.4 mW	/ 1 pt.

Q14: ESTIMATE THE POWER LOSSES OF THE GATE DRIVER

Refer to section 8.2.2.3 of the datasheet to calculate the loss components in the gate driver device. Report calculation procedure in the framed box. Then, sum them to obtain the estimated total loss of the gate driver and report it below.
Note: The gate driver internal pull up/down resistor can be calculated as (8). The average value of pull-up and pull-down resistor,$R_{GD\text{-}R}$, is 4.1Ω ,

High-side pull-up resistor:	$R_{HOH} = V_{HOH}/I_{HO}$	= 0.42V/100mA = 4.2Ω
High-side pull-down resistor:	$R_{HOL} = V_{HOL}/I_{HO}$	= 0.40V/100mA = 4.0Ω
Low-side pull-up resistor:	$R_{LOH} = V_{LOH}/I_{LO}$	= 0.42V/100mA = 4.2Ω
Low-side pull-down resistor:	$R_{LOL} = V_{LOL}/I_{LO}$	= 0.40V/100mA = 4.0Ω

(4)

Using equations from the datasheet, with $V_{DD} = 12\,V$, $V_{DH} = 0.9\,V$, $Q_G = 25\,nC$, $f_{sw} = 250\,kHz$, $R_{GD\text{-}R} = 4.1\,\Omega$, $R_{GATE} = 10\,\Omega$, $R_{GFET(int)} = 2\,\Omega$, $D = 0.5$, $V_{HB} = V_{in,max} + (V_{DD} - V_{DH}) = 60 + 11.1 = 71.1\,V$.
1. Quiescent static losses ($I_{DD,max} = 0.45\,mA$, $I_{HB,max} = 0.4\,mA$):

$$P_{QC} = (V_{DD} \times I_{DD,max}) + (V_{DD} - V_{DH}) \times I_{HB,max} = (12 \times 0.45\,mA) + (11.1 \times 0.40\,mA) = 9.84\,mW$$

2. Level-shifter leakage ($I_{HBS,max}$ = 50 μA):

$$P_{IHBS} = V_{HB} \times I_{HBS,max} \times D = 71.1 \times 50 \times 10^{-6} \times 0.5 = 1.78\,\text{mW}$$

3. Dynamic gate-charge losses:

$$P_{QG} = 2 \times V_{DD} \times Q_G \times f_{sw} \times \frac{R_{GD\text{-}R}}{R_{GD\text{-}R} + R_{GATE} + R_{GFET(int)}} = 2 \times 12 \times 25\,\text{nC} \times 250\,\text{kHz} \times \frac{4.1}{16.1} = 38.2\,\text{mW}$$

4. Level-shifter dynamic losses (Q_P = 1 nC assumed):

$$P_{LS} = V_{HB} \times Q_P \times f_{sw} = 71.1 \times 1\,\text{nC} \times 250\,\text{kHz} = 17.8\,\text{mW}$$

$$P_{driver} = P_{QC} + P_{IHBS} + P_{QG} + P_{LS} = 9.84 + 1.78 + 38.2 + 17.8 = 67.6\,\text{mW}$$

P_{driver} = 67.6 mW

/ 3 pt.

Q15: CALCULATE MAXIMUM ALLOWED POWER DISSIPATION IN THE GATE DRIVER DEVICE

Refer to section 8.2.2.3 of the datasheet and calculate the maximum allowed power dissipation in the gate driver device. Here, the ambient temperature is set as 50℃.

P_{max} = 0.76 W

/ 1 pt.

GATE DRIVER ON THE SECONDARY SIDE

As mentioned, the design of the gate driver circuit depends on the MOSFET. Therefore, the design for the gate driver on the secondary will be different from that of the primary side.

Q16: CALCULATION OF THE BOOTSTRAP CAPACITOR

Refer to section 8.2.2.1 of the UCC27288 datasheet, and calculate the capacitance of the bootstrap capacitor following the step-by-step procedure. Report calculation procedure in the framed box, and calculated values in the answer boxes. Then, choose the closest standard capacitance value (see the Appendix), and report selected capacitor and its voltage rating in the answer boxes.
Note: In this calculation, forward voltage drop over the diode, D_{Boot}, is about 0.9 V. VDD is 12 V.

The secondary side uses the same UCC27288 with
$V_{DD} = 12\,\text{V}$, $V_{DH} = 0.9\,\text{V}$, $Q_{g,sec} = 23\,\text{nC}$, $f_{sw} = 250\,\text{kHz}$, $D_{MAX} = 0.5$.
The following stay unchanged: $V_{HBR(max)} = 7.1\,\text{V}$, $V_{HBHys} = 0.5\,\text{V}$.

$$\Delta V_{HB} = V_{DD} - V_{DH} - (V_{HBR(max)} - V_{HBHys}) = 12 - 0.9 - (7.1 - 0.5) = 4.5\,\text{V}$$

$$Q_{TOTAL} = Q_G + I_{HBS,max} \times \frac{D_{MAX}}{f_{SW}} + \frac{I_{HB}}{f_{SW}} = 23 \times 10^{-9} + 50 \times 10^{-6} \times \frac{0.5}{250 \times 10^3} + \frac{0.4 \times 10^{-3}}{250 \times 10^3} = 24.7 \times 10^{-9}\,\text{C}$$

$$C_{boot,min} = \frac{Q_{TOTAL}}{\Delta V_{HB}} = \frac{24.7 \times 10^{-9}}{4.5} = 5.49\,\text{nF}$$

Same as the primary side, we select the **C1206C683J1RECAUTO** capacitor that has ($C_{\text{boot,selected}}$, $V_{\text{Cboot,rated}}$) = (68 *nF*, 100*V*) and X7R dielectric.
This satisfies $C_{boot,selected} \gg C_{boot,min}$ and the voltage rating $100\,\text{V} \gg 2 \times V_{Cboot,max} = 2 \times (V_{DD} - V_{DH}) = 2 \times 11.1 = 22.2\,\text{V}$, as required by the datasheet.

$\Delta V_{\text{HB}} = 4.5\,\text{V}$ | $Q_{\text{TOTAL}} = 24.7 \times 10^{-9}\,\text{C}$ | $C_{\text{boot,min}} = 5.49 \times 10^{-9}\,\text{F}$
$C_{\text{boot,selected}} = 68 \times 10^{-9}\,\text{F}$ | $V_{\text{Cboot,rated}} = 100\,\text{V}$ | / 3 pt.

Q17: SELECTION OF THE VDD CAPACITOR

Refer to section 8.2.2.1 of the UCC27288 datasheet, and calculate the required VDD capacitor. Then, choose the closest standard capacitance value (see the Appendix). Report selected capacitor and its voltage rating in the answer boxes.

Following the same rule as the primary side, the VDD capacitor must be at least 10 times the bootstrap capacitor value, and its voltage rating must exceed $2 \times V_{DD} = 24\,\text{V}$, with X7R dielectric.

$$C_{VDD,min} = 10 \times C_{boot,selected} = 10 \times 68\,\text{nF} = 680\,\text{nF}$$

We select the **C1206C105K3RACTU** $C_{VDD} = 1\,\mu\text{F}$, $V_{rated} = 25\,\text{V}$, X7R. This satisfies $1\,\mu\text{F} > 680\,\text{nF}$ and $25\,\text{V} > 24\,\text{V}$.

$C_{\text{VDD,selected}} = 1\,\mu\text{F}$ | $V_{\text{CVDD,rated}} = 25\,\text{V}$ | / 2 pt.

Q18: SELECTION OF THE BOOTSTRAP SERIES RESISTOR

The series resistance R_{boot} will limit the peak current at the bootstrap diode during start-up, but it should also be carefully selected as it introduces a time constant with the bootstrap capacitor given by

$$\tau = R_{\text{boot}} C_{\text{boot}}. \tag{5}$$

This time constant is related to the start-up time, which influences the load dv/dt. In this project, the selected R_{boot} should satisfy

$$3R_{\text{boot}} C_{\text{boot}} < 10 D_{\text{min}} / f_{\text{sw}}. \tag{6}$$

where D_{min} is set to 0.05.
Additionally, the chosen bootstrap resistor must be able to withstand high power dissipation during the first charging sequence of the bootstrap capacitor. This energy and average power can be estimated by

$$E_{boot} = \frac{1}{2} C_{boot} V_{boot}^2, \quad P_{R(boot)} = E_{boot} \cdot f_{sw} \tag{7}$$

In this specific project course, we suggest that R_{boot} be in the range of 1 Ω to 10 Ω. Choose a proper package for this resistor.

Added box
Using $C_{boot} = 68\,\text{nF}$, $D_{min} = 0.05$, $f_{sw} = 250\,\text{kHz}$, the time-constant constraint gives:

$$R_{boot} < \frac{10\,D_{min}}{3\,f_{sw}\,C_{boot}} = \frac{10 \times 0.05}{3 \times 250 \times 10^3 \times 68 \times 10^{-9}} = 9.80\,\Omega$$

We select $R_{boot} = 4.99\,\Omega$ (RMCF1206FT4R99), within the suggested 1–10 Ω range. Verification:

$$3\,R_{boot}\,C_{boot} = 3 \times 4.99 \times 68 \times 10^{-9} = 1.02\,\mu\text{s} < 2.0\,\mu\text{s}\checkmark$$

The bootstrap capacitor charges to $V_{boot} = V_{DD} - V_{DH} = 12 - 0.9 = 11.1\,\text{V}$. The power dissipated in R_{boot} during the first charging sequence is:

$$P_{R(boot)} = \frac{1}{2}\,C_{boot}\,V_{boot}^2\,f_{sw} = \frac{1}{2} \times 68 \times 10^{-9} \times 11.1^2 \times 250 \times 10^3 = 1.05\,\text{W}$$

Since this exceeds the 0.25 W rating of a 1206 package, a higher power package (2512 or through-hole) must be used for this resistor. Note that this dissipation occurs only during the brief start-up transient, not in steady state.

R_{boot} = 4.99 Ω	$P_{R(boot)}$ = 1.05 W	/ 2 pt.

Q19: CALCULATE THE VOLTAGE STRESS AND PEAK CURRENT OVER THE BOOTSTRAP DIODE

When the high-side device is on, the bootstrap diode will be reverse-biased. The selection of the bootstrap diode should consider the voltage stress and peak current through the diode during the start-up charging.

In this project course, the ES2C diode will be used as the bootstrap diode.

Added box
Peak inrush current through D_{boot} during start-up, when C_{boot} is uncharged and the low-side first conducts:

$$I_{Dboot,peak} = \frac{V_{DD} - V_{DH}}{R_{boot}} = \frac{12 - 0.9}{4.99} = \frac{11.1}{4.99} = 2.22\,\text{A}$$

Peak reverse voltage across D_{boot} when the high-side MOSFET conducts. On the secondary side the switch node (HS) rises to $V_{out} = 24\,\text{V}$. Since the bootstrap capacitor voltage is fixed at $V_{Cboot} = V_{DD} - V_{DH} = 11.1\,\text{V}$, the HB node rises to:

$$V_{HB} = V_{HS} + V_{Cboot} = 24 + 11.1 = 35.1\,\text{V}$$

The diode anode is at $V_{DD} = 12\,\text{V}$, so the reverse voltage is:

$$V_{Dboot,peak} = V_{HB} - V_{DD} = V_{out} + V_{Cboot} - V_{DD} = 24 + 11.1 - 12 = 23.1\,\text{V}$$

The ES2C diode ($V_{RRM} = 150\,\text{V}$) comfortably withstands this stress. Note that compared to the primary side ($V_{Dboot,peak} = 59.1\,\text{V}$), the secondary stress is significantly lower since $V_{out} = 24\,\text{V} \ll V_{in,max} = 60\,\text{V}$.

$V_{Dboot,peak}$ = 23.1 V	$I_{Dboot,peak}$ = 2.22 A	/ 1 pt.

Q20: SELECTION OF THE EXTERNAL GATE RESISTOR

In gate drivers for high-frequency converters, parasitic inductance and parasitic capacitance can cause voltage and current oscillations on the gate of the power MOSFETs. These oscillations can cause the breakdown of the device and disturb adjacent circuits. External gate resistors are typically used to slow down the turn-on and turn-off of the devices, thus mitigating these oscillations. Refer

to Section 8.2.2.4, select the external gate resistor, and calculate the source and sink current of the gate driver. In this project course, we suggest that the external gate resistor is in the range of 5 Ω to 10 Ω.

Note: In the practical experimental test, you should capture waveform of the gate-source voltage. If there are obvious oscillations which may result in fault switching on, i.e., the amplitude of the oscillations higher than he turn-on threshold, the resistor should be increased.

The secondary side uses the same UCC27288 with the same MOSFETs (PHP18NQ11T), so V_{DD} = 12 V, V_{DH} = 0.9 V, and $R_{GFET(int)}$ = 2 Ω. The gate currents depend only on V_{DD}, V_{DH}, and the resistances, which are all identical to the primary side. We therefore select the same R_{GATE} = 10 Ω (RMCF1206FT10R0), the only individual resistor available in the required 5–10 Ω range.

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{GATE} + R_{GFET(int)}} = \frac{12 - 0.9}{4.2 + 10 + 2} = \frac{11.1}{16.2} = 0.685\,\text{A}$$

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{GATE} + R_{GFET(int)}} = \frac{11.1}{4.0 + 10 + 2} = \frac{11.1}{16.0} = 0.694\,\text{A}$$

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{GATE} + R_{GFET(int)}} = \frac{12}{4.2 + 10 + 2} = \frac{12}{16.2} = 0.741\,\text{A}$$

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{GATE} + R_{GFET(int)}} = \frac{12}{4.0 + 10 + 2} = \frac{12}{16.0} = 0.750\,\text{A}$$

All currents are below the ±3 A peak rating of the UCC27288.

R_g = 10 Ω	I_{OHH} = 0.685 A	I_{OLH} = 0.694 A	I_{OHL} = 0.741 A	I_{OLL} = 0.750 A	/ 2 pt.

Q21: SELECTION OF THE EXTERNAL GATE-SOURCE RESISTOR

The gate-source resistor (often called a pull-down resistor for N-channel devices) is a crucial safety component in MOSFET circuits. It prevents the MOSFET from turning on accidentally when the control signal is disconnected or undefined.
For most power electronics applications (Motor drives, DC-DC converters), the standard value lies between 5 kΩ and 15 kΩ.
Select a reasonable resistance value R_{gs} and calculate the expected power dissipation P_{Rgs}.

We select R_{gs} = 10 kΩ (RMCF1206FT10K0), within the standard 5–15 kΩ range for power electronics applications.
The peak power dissipation occurs when the gate is fully driven to V_{DD} = 12 V:

$$P_{Rgs} = \frac{V_{DD}^2}{R_{gs}} = \frac{12^2}{10 \times 10^3} = \frac{144}{10000} = 14.4\,\text{mW}$$

This is well below the 0.25 W rating of the 1206 package.

R_{gs} = 10 kΩ	P_{Rgs} = 14.4 mW	/ 1 pt.

Q22: ESTIMATE THE POWER LOSSES OF THE GATE DRIVER

Refer to section 8.2.2.3 of the datasheet to calculate the loss components in the gate driver device. Report the calculation procedure in the framed box as outlined in the datasheet. Then, sum them to obtain the estimated total loss of the gate driver and report it below. **Note:** The gate driver internal pull up/down resistor can be calculated as in (8). The average value of the pull-up and pull-down resistors, $R_{GD\text{-}R}$, is 4.1 Ω since

High-side pull-up resistor:	$R_{HOH} = V_{HOH}/I_{HO}$	= 0.42V/100mA = 4.2 Ω
High-side pull-down resistor:	$R_{HOL} = V_{HOL}/I_{HO}$	= 0.40V/100mA = 4.0 Ω
Low-side pull-up resistor:	$R_{LOH} = V_{LOH}/I_{LO}$	= 0.42V/100mA = 4.2 Ω
Low-side pull-down resistor:	$R_{LOL} = V_{LOL}/I_{LO}$	= 0.40V/100mA = 4.0 Ω

(8)

Using the equations from the datasheet, with $V_{DD} = 12\,\text{V}$, $V_{DH} = 0.9\,\text{V}$, $Q_G = 23\,\text{nC}$, $f_{sw} = 250\,\text{kHz}$, $R_{GD\text{-}R} = 4.1\,\Omega$, $R_{GATE} = 10\,\Omega$, $R_{GFET(int)} = 2\,\Omega$, $D = 0.5$.
On the secondary side the switch node rises to $V_{out} = 24\,\text{V}$, so $V_{HB} = V_{out} + V_{Cboot} = 24 + 11.1 = 35.1\,\text{V}$.

1. **Quiescent static losses** ($I_{DD,max} = 0.45\,\text{mA}$, $I_{HB,max} = 0.4\,\text{mA}$):

$$P_{QC} = (V_{DD} \times I_{DD,max}) + (V_{DD} - V_{DH}) \times I_{HB,max} = (12 \times 0.45\,\text{mA}) + (11.1 \times 0.40\,\text{mA}) = 9.84\,\text{mW}$$

2. **Level-shifter leakage** ($I_{HBS,max} = 50\,\mu\text{A}$):

$$P_{IHBS} = V_{HB} \times I_{HBS,max} \times D = 35.1 \times 50 \times 10^{-6} \times 0.5 = 0.88\,\text{mW}$$

3. **Dynamic gate-charge losses** (factor 2 for both HS and LS MOSFETs):

$$P_{QG} = 2 \times V_{DD} \times Q_G \times f_{sw} \times \frac{R_{GD\text{-}R}}{R_{GD\text{-}R} + R_{GATE} + R_{GFET(int)}} = 2 \times 12 \times 23\,\text{nC} \times 250\,\text{kHz} \times \frac{4.1}{16.1} = 35.2\,\text{mW}$$

4. **Level-shifter dynamic losses** ($Q_P = 1\,\text{nC}$ assumed):

$$P_{LS} = V_{HB} \times Q_P \times f_{sw} = 35.1 \times 1\,\text{nC} \times 250\,\text{kHz} = 8.78\,\text{mW}$$

$$P_{driver} = P_{QC} + P_{IHBS} + P_{QG} + P_{LS} = 9.84 + 0.88 + 35.2 + 8.78 = 54.7\,\text{mW}$$

This is lower than the primary side (67.6 mW) because both $Q_{g,sec}$ and V_{HB} are smaller on the secondary side.

P_{driver} = 54.7 mW

/ 3 pt.

Q23: CALCULATE MAXIMUM ALLOWED POWER DISSIPATION IN THE GATE DRIVER DEVICE

Refer to section 8.2.2.3 of the datasheet and calculate the maximum allowed power dissipation in the gate driver device. Here, the ambient temperature is to be set as 40℃.

Added box

Using Equation (8) from section 8.2.2.3 of the datasheet, with the maximum recommended junction temperature $T_{J,max} = 140\,^{\circ}\text{C}$, ambient temperature $T_A = 40\,^{\circ}\text{C}$, and junction-to-ambient thermal resistance $R_{\theta JA} = 118.3\,^{\circ}\text{C/W}$ (from the Thermal Information table):

$$P_{max} = \frac{T_{J,max} - T_A}{R_{\theta JA}} = \frac{140 - 40}{118.3} = \frac{100}{118.3} = 0.845\,\text{W}$$

Since $P_{driver} = 54.7\,\text{mW} \ll P_{max} = 0.845\,\text{W}$, the gate driver operates safely within its thermal limits.

P_{max} = 0.845 W

/ 1 pt.

Q24: CALCULATE PWM SIGNALS LOW-PASS FILTER FOR BOTH PRIMARY AND SECONDARY SIDE

In order to filter the noise induced by the parasitic inductance and capacitance of the cable connection between the power stage and the controller, a first-order low-pass filter (LPF) is suggested, as shown in Fig. 4. To filter out the noise while maintaining the main signal intact, the cut-off frequency of the low-pass filter could be set approximately to 50 times the switching frequency. In addition, it should be considered that the maximum current that can be drawn from the circuit at the input of the low-pass filter is 2 mA (hint: the maximum current is limited by the resistor). The complex-valued transfer function is expressed as a function of frequency f in (9) (j is the imaginary unit, R_{LPF} and C_{LPF} are the resistor and the capacitor of the LPF, respectively). Design the low-pass filter and plot the transfer function (i.e., the Bode plot) of this filter, also indicating with vertical lines your switching frequency and the designed cut-off frequency.

$$\frac{v_{\text{out,LPF}}(f)}{v_{\text{in,LPF}}(f)} = \frac{1}{j(2\pi f)R_{\text{LPF}}C_{\text{LPF}} + 1} \tag{9}$$

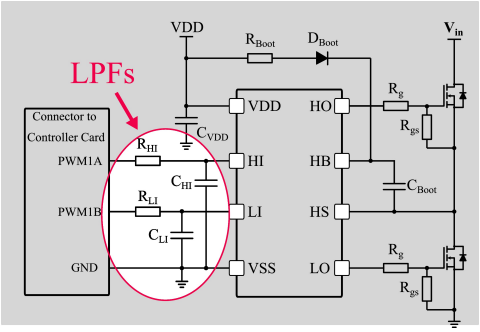


Figure 4 First-order low pass filters for the PWM signals.

The PWM signals are 3.3 V logic signals from the DSP controller. The maximum current constraint limits the minimum resistance:

$$R_{LPF} \geq \frac{V_{high}}{I_{max}} = \frac{3.3\,\text{V}}{2\,\text{mA}} = 1.65\,\text{k}\Omega$$

We select the closest available E96 value from KIT-RMCF1206FT-04: $R_{HI} = R_{LI} = 1.65\,\text{k}\Omega$.

The target cut-off frequency is:

$$f_{cutoff,target} = 50 \times f_{sw} = 50 \times 250\,\text{kHz} = 12.5\,\text{MHz}$$

The required capacitance for this target would be:

$$C = \frac{1}{2\pi \times R_{LPF} \times f_{cutoff,target}} = \frac{1}{2\pi \times 1650 \times 12.5 \times 10^{6}} = 7.72\,\text{pF}$$

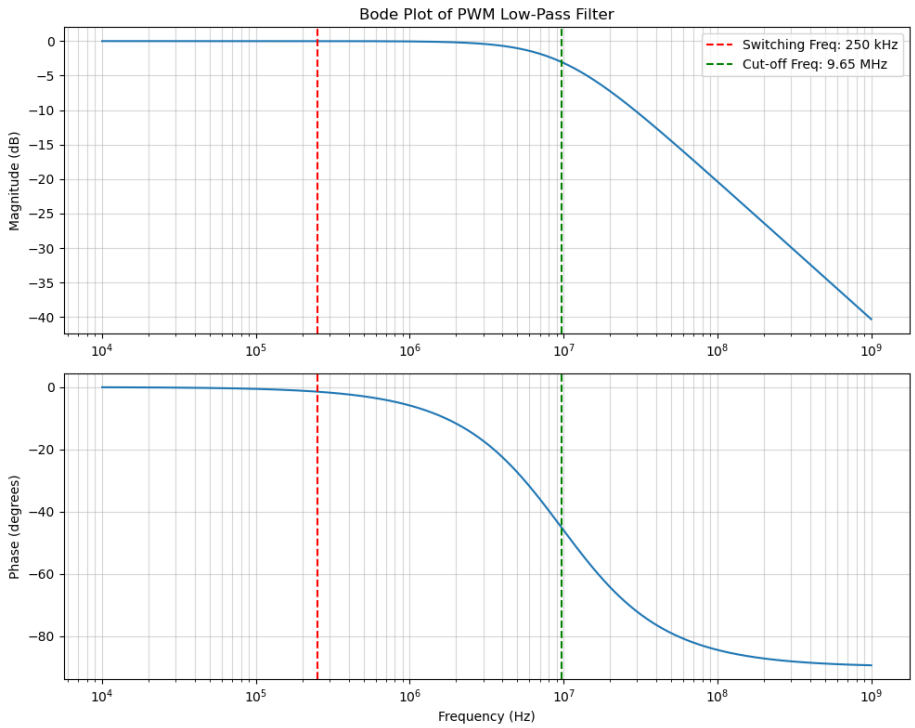
This value is not available in the component list. The smallest available capacitor is 10 pF (C1206C100J2GACTU), so we select $C_{HI} = C_{LI} = 10\,\text{pF}$. The resulting cut-off frequency is:

$$f_{cutoff} = \frac{1}{2\pi \times R_{LPF} \times C_{LPF}} = \frac{1}{2\pi \times 1.65 \times 10^{3} \times 10 \times 10^{-12}} = 9.65\,\text{MHz} \approx 38.6 \times f_{sw}$$

This is the best achievable value: reducing R further would result in a current greater than the 2 mA current limit, and no smaller standard capacitor is available. The filter still provides strong attenuation well above the switching frequency while passing the PWM signal with negligible distortion.
The same component values apply to both the HI and LI inputs, and identically to both the primary and secondary side gate drivers, since all four PWM channels originate from the same 3.3 V controller.
The transfer function magnitude and phase are:

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{\sqrt{1 + (2\pi f \cdot R_{LPF} \cdot C_{LPF})^2}}, \qquad \angle\frac{V_{out}}{V_{in}} = -\arctan(2\pi f \cdot R_{LPF} \cdot C_{LPF})$$

At $f_{sw} = 250\,\text{kHz}$: attenuation = 0.026 dB, phase shift = -1.49° – the PWM signal passes essentially undistorted.
At $f_{cutoff} = 9.65\,\text{MHz}$: attenuation = –3 dB.



R_{HI} = 1.65 kΩ | $C_{HI} = 10 \times 10^{-12}$ F | R_{LI} = 1.65 kΩ | $C_{LI} = 10 \times 10^{-12}$ F | f_{cutoff} = 9.65 $\times 10^{6}$ Hz | / 2 pt.

CURRENT MEASUREMENT

Current sensing is necessary to protect the hardware from over-current damage and to precisely control how power is delivered to the load. In this project, current sensing is used only for safety and protection via the digital controller, i.e., the digital signal processor (DSP). A sensing circuit is thus needed to convert the electrical quantity being measured into a form that the micro-controller can read. In this course, the **INA201AIDR** from Texas Instruments and a shunt resistor are used for current measurements. The typical circuit is shown in Fig.5. When the current amplitude needs to be acquired by the DSP, the "OUT" pin of the IC should be connected to one of the inputs of the analog-to-digital converter (ADC) of the digital controller. In this case, the information of the amplitude of the current can be used for both control and protection purposes in the control software executed on the DSP. When only an over-current alert is needed (i.e., a digital signal for protection), the "OUT" pin can be connected to "CMPin" via a voltage divider, then compared with an internal 0.6 V reference through the internal comparator in the INA20X. The alert threshold can be configured using the voltage divider.

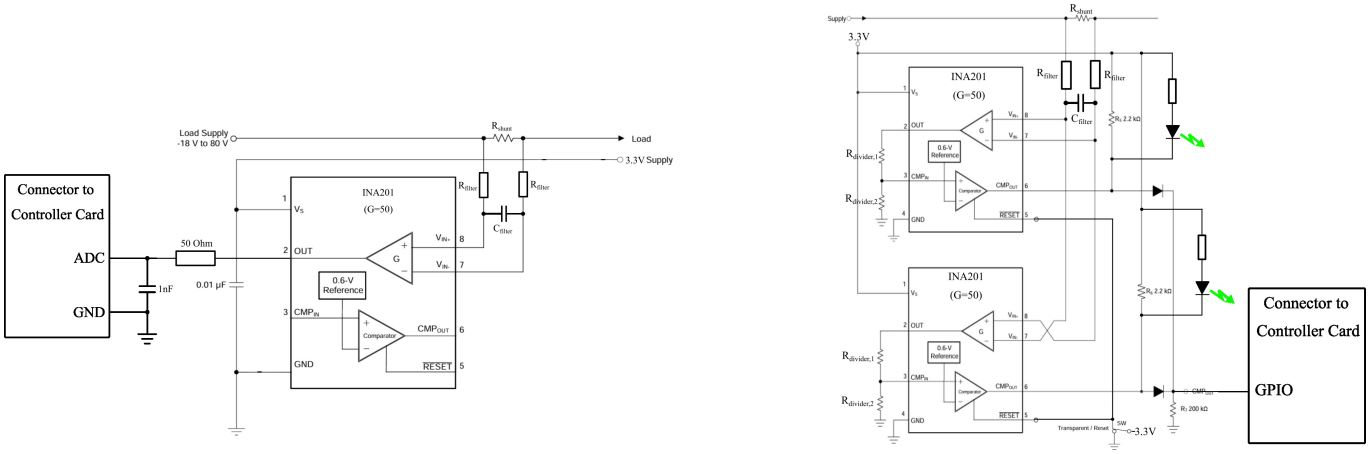


Figure 5 Typical application circuit of the INA201 and shunt resistor. On the left, the analog signal representing the current being measured is acquired by the digital controller (uC) through one of the analog-to-digital (ADC) inputs. On the right, the current measurement is used only for protection; therefore, the measurement is fed to the comparator through a voltage divider, and ultimately read by one of the GPIO pins (configured as a digital input) of the micro-controller.

In this project, the DC input current and output current should be sensed and measured with the digital controller, while the DAB inductor current should only be monitored to avoid over-current. This means that if an over-current event occurs in the inductor, the comparator should output a digital "high" value and send a signal to the digital controller to shut down the PWM output.

Note: There is a detailed design example in the datasheet of the INA201. Please read it carefully at this **LINK**.
Note: The supply voltage for the INA201, V_S, is set to 3.3 V.
Note: Generally, it is a good engineering practice to have the digital signals for fault detection as "active low" (i.e., the signal is in state "high" when the protection is not needed, while it is in state "low" when the protection is needed). In this project, instead, we use the "active high" logic to simplify the circuit.

Q25: ESTIMATE COMMON MODE VOLTAGE OVER THE THE CURRENT-SENSE AMPLIFIER

Refer to Fig. 1. According to the position of the primary and secondary shunt resistors and current-sense amplifiers, estimate the common-mode (CM) voltage stress across the current-sense amplifiers at the primary and secondary side.

Note: Common-mode voltage ($V_{CM,pri(sec)}$) is the average voltage present on both inputs of a differential circuit (such as an op-amp) relative to a common reference point, usually ground.

$V_{CM,pri}$ = 50 V	$V_{CM,sec}$ = 24 V	/ 1 pt.

Q26: SELECTION OF SHUNT RESISTORS

To sense the input and output current, the "OUT" pin needs to connect to the ADC input of the digital controller. Considering that the allowable input range for the ADC of the selected digital controller ranges from 0 V to 3 V, the voltage of the "OUT" pin should be below 3 V. Since the voltage gain of the INA201 is 50 V/V, the voltage across the shunt resistor should be below 60 mV.
To ensure that the voltage of the shunt resistors are not exceeding 50 mV, a 40% margin should be considered. Therefore, the selection of the shunt resistor should follow the equation below. The list of the available shunt resistors can be found in the Appendix.

$$1.4 \cdot R_{shunt,pri,max} \cdot I_{in,max} \leq 60mV, \qquad 1.4 \cdot R_{shunt,sec,max} \cdot I_{out,max} \leq 60mV \tag{10}$$

This equations represent the upper bounds for the resistance values. Besides, the resistors should not be much smaller because this will reduce the voltage range representing the current signals. For sake of simplicity, the shunt resistor for the inductor current can be selected using the same criterion.
For the used digital controller, TMS320F28335, the resolution for the ADC is 12 bit. The digital value of the input analog voltage at ADC terminal can be derived by (11). And it should be noted that all fractional values are truncated. Combine the selected shunt resistor and voltage gain of the INA201, calculate the digital value (DV) get from controller for the rated input and output current, and report them in the answer boxes.

$$\text{Digital Value} = 2^{12} \cdot \frac{\text{Input Analog Voltage} - 0}{3} \tag{11}$$

- **Primary shunt** $R_{shunt,pri}$ (measures DC input current i_{in}):
  Maximum DC input current at minimum input voltage:

$$I_{in,max} = \frac{P_{out}}{V_{in,min}} = \frac{50\,\text{W}}{30\,\text{V}} = 1.667\,\text{A}$$

$$R_{shunt,pri} \le \frac{60\,\text{mV}}{1.4 \times I_{in,max}} = \frac{60 \times 10^{-3}}{1.4 \times 1.667} = 25.7\,\text{m}\Omega$$

  We select **CSNL2512FT25L0**: $R_{shunt,pri} = 25\,\text{m}\Omega$, rated 3 W.
  Then we get:

$$P_{Rshunt,pri} = I_{in,max}^2 \times R_{shunt,pri} = (1.667)^2 \times 25 \times 10^{-3} = 69.5\,\text{mW} \ll 3\,\text{W}$$

  Digital value at rated operating point ($V_{in,nom} = 50\,\text{V}$, $I_{in,rated} = P_{out}/V_{in,nom} = 50/50 = 1\,\text{A}$). The INA201 gain is 50 V/V, so $V_{OUT} = I \times R \times 50$:

$$V_{OUT} = 1\,\text{A} \times 25\,\text{m}\Omega \times 50 = 1.25\,\text{V}$$

$$DV_{I,rated,in} = \left\lfloor 4096 \times \frac{1.25}{3} \right\rfloor = \lfloor 1706.7 \rfloor = 1706$$

- **Secondary shunt** $R_{shunt,sec}$ (measures DC output current i_{out}):
  Maximum DC output current:

$$I_{out,max} = \frac{P_{out}}{V_{out}} = \frac{50\,\text{W}}{24\,\text{V}} = 2.083\,\text{A}$$

$$R_{shunt,sec} \le \frac{60 \times 10^{-3}}{1.4 \times 2.083} = 20.6\,\text{m}\Omega$$

  We select **CSNL2512FT20L0**: $R_{shunt,sec} = 20\,\text{m}\Omega$, rated 3 W.
  Then we get:

$$P_{Rshunt,sec} = I_{out,max}^2 \times R_{shunt,sec} = (2.083)^2 \times 20 \times 10^{-3} = 86.8\,\text{mW} \ll 3\,\text{W}$$

  Digital value at rated output current ($I_{out,rated} = 2.083\,\text{A}$):

$$V_{OUT} = 2.083\,\text{A} \times 20\,\text{m}\Omega \times 50 = 2.083\,\text{V}$$

$$DV_{I,rated,out} = \left\lfloor 4096 \times \frac{2.083}{3} \right\rfloor = \lfloor 2845.9 \rfloor = 2845$$

- **AC inductor shunt** $R_{shunt,ac}$ (measures inductor current i_L for over-current protection):
  The peak inductor current is the worst-case sizing current (Report 1, at $V_{in,min}$): $I_{L,peak} = I_1 = 3.6\,\text{A}$

$$R_{shunt,ac} \le \frac{60 \times 10^{-3}}{1.4 \times 3.6} = 11.9\,\text{m}\Omega$$

  We select **CSNL2512FT10L0**: $R_{shunt,ac} = 10\,\text{m}\Omega$, rated 2 W.
  Power dissipation using $I_{L,rms} = 2.08\,\text{A}$ (Report 1):

$$P_{Rshunt,ac} = I_{L,rms}^2 \times R_{shunt,ac} = (2.08)^2 \times 10 \times 10^{-3} = 43.3\,\text{mW} \ll 2\,\text{W}$$

  No digital value is required for this shunt as it is used only for over-current protection via the comparator, not ADC acquisition.

$R_{\text{shunt,pri}}$ = 25 mΩ	$P_{\text{Rshunt,pri}}$ = 69.5 mW	$\text{DV}_{\text{I,rate,in}}$ = 1706
$R_{\text{shunt,sec}}$ = 20 mΩ	$P_{\text{Rshunt,sec}}$ = 86.8 mW	$\text{DV}_{\text{I,rate,out}}$ = 2845

$R_{shunt,ac}$ = 10 mΩ	$P_{Rshunt,ac}$ = 43.3 mW	/ 4 pt.

Q27: FILTER DESIGN FOR INPUT AND OUTPUT CURRENT SENSING

To filter the switching frequency noise when sensing the input and output DC current, it is suggested to add a low pass filter as shown in Fig.6.

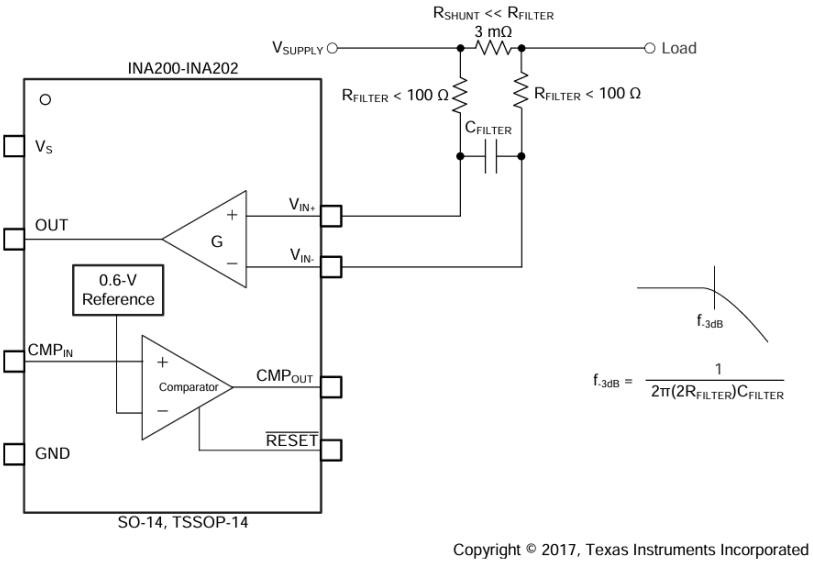


Figure 6 Circuit diagram of input filter applied to a component of the INA20x series.

Decide a reasonable cut-off frequency of this input filter according to the switching frequency, usually the cut-off frequency is 1/20 to 1/10 of the switching frequency, and then select the corresponding R_{filter} and C_{filter}.

The cut-off frequency should lie between $f_{sw}/20$ and $f_{sw}/10$:

$$f_{c,target} \in \left[\frac{250\,\text{kHz}}{20}, \frac{250\,\text{kHz}}{10}\right] = [12.5\,\text{kHz},\ 25\,\text{kHz}], \quad \text{and} \quad f_{3dB} = \frac{1}{2\pi\,(2 \times R_{filter})\,C_{filter}}$$

From Fig. 6 from the **INA201 datasheet**, we can see that: $R_{filter} < 100\,\Omega$ and $R_{shunt} \ll R_{filter}$.
We select the resistors from the **KIT-RMCF1206FT-05**: $R_{filter} = 51.1\,\Omega$ and the capacitor **C1206C683J1RECAUTO**: $C_{filter} = 68\,\text{nF}$ (already used in the design).

$$f_{cutoff} = \frac{1}{2\pi \times 2 \times 51.1 \times 68 \times 10^{-9}} = 22.9\,\text{kHz} \in [12.5\,\text{kHz},\ 25\,\text{kHz}]$$

The same component values apply to both the primary and secondary sides since both measure DC currents at the same switching frequency.

$f_{cut-off,pri}$ = 22.9 ×10^3 Hz	$R_{filter,pri}$ = 51.1 Ω	$C_{filter,pri}$ = 68 ×10^{-9} F	
$f_{cut-off,sec}$ = 22.9 ×10^3 Hz	$R_{filter,sec}$ = 51.1 Ω	$C_{filter,sec}$ = 68 ×10^{-9} F	/ 2 pt.

Q28: INDUCTOR CURRENT MONITORING CIRCUIT FOR PROTECTION

In this project, the current of the DAB inductor needs to be monitored. When there is an over-current fault, a digital fault signal should be generated by the current sensing circuit and sent to the digital controller to shut down the PWM.
The INA201 current-sense amplifier includes a comparator and an internal 0.6 V voltage reference. Refer to section 7.3.3 to understand the operating principle of the over-current protection.

The design of the voltage divider should consider the following equation:

$$I_{L,alert,threshold} = \frac{0.6\text{V} \cdot (R_{divider,1} + R_{divider,2})}{R_{shunt,ac} \cdot \text{Gain} \cdot R_{divider,2}}, \tag{12}$$

where Gain is the voltage gain of the INA201, $I_{\text{L,alert,threshold}}$ is the inductor over-current threshold (which is set to 140% of the calculated maximum inductor current). Here, we suggest that $R_{\text{divider,2}}$ is fixed to 10 kΩ. And $R_{\text{divider,1}}$ uses a potentiometer in series with a resistor. The maximum resistance of the potentiometer is 10kOhm.

The over current detection circuit is shown in Fig. 5 (right figure). Additionally, refer to Fig. 6, adding a filter in the over current detection circuit as well. It should be noted that to keep switching-frequency information, the cut-off frequency of the low-pass filter is 20 times higher than the switching frequency. It should also be noted that the "RESET" pin is connected to a push button, which is normally tied to 3.3V, meaning that the fault signal will be latched. To reset the signal, push the button to have the "RESET" pin connected to ground. To protect the IC, two diodes are used in this circuit. In this project, diode ES2C is asked to be used.

The maximum inductor current is $I_{L,peak} = 3.6$ A. Then $I_{\text{L,alert,threshold}} = I_{L,peak} \times 1.4 = 5.04$ A and the gain of the the INA201 is Gain=$50V/V$.

By fixing $R_{\text{divider-2}}$ to 10kΩ, we can find the value of $R_{\text{divider-1}}$:

$$I_{\text{L,alert,threshold}} = \frac{0.6\text{V} \cdot (R_{\text{divider,1}} + R_{\text{divider,2}})}{R_{\text{shunt,ac}} \cdot \text{Gain} \cdot R_{\text{divider,2}}},$$

$$R_{\text{divider,1}} = \frac{I_{\text{L,alert,threshold}} \cdot R_{\text{shunt,ac}} \cdot \text{Gain} \cdot R_{\text{divider,2}}}{0.6\text{V}} - R_{\text{divider,2}} = \frac{5.04A \cdot 10m\Omega \cdot 50V/V \cdot 10k\Omega}{0.6\text{V}} - 10k\Omega = 32k\Omega$$

As stated we choose a **10 kΩ potentiometer** in series with a 25.5 kΩ from the KIT-RMCF1206FT-05. This allows us to have $R_{\text{divider,1}} \in [25.5\,;35.5]$ kΩ. We choose a **RMCF1206FT10K0** (10 kΩ) resistor for $R_{\text{divider-2}}$

$I_{\text{L,alert,threshold}}$ = 5.04 A	$R_{\text{divider-1}}$ = 32 kΩ	$R_{\text{divider-2}}$ = 10 kΩ	/ 2 pt.

Q29: CALCULATE THE CURRENT-LIMITING RESISTOR OF THE LED

Refer to the right figure in Fig. 5, a green LED in series with a resistor is connected between the "CMPout" pin and the Vs supply pin. When the inductor current is below the alert level, the "CMPout" pin is LOW, and the green LED will be ON to represent a normal working status. When the inductor current is above the alert threshold level, "CMPout" pin is HIGH, and the green LED will be OFF. To limit the current through the LED, a resistor is needed.
Here is the **LINK** of the datasheet of the LED. Select the proper limiting resistor to limit the current through the LED is around 2 mA. And calculate the power consumption of the LED circuit.

Added box

$$R_{LED} = \frac{3.3V - 1.9V}{2mA} = 700\Omega$$

We choose the closest available resistance of 680 Ω(**RMCF1206FT680R**)
The current in the branch is: $I_{Led} = \frac{3.3-1.9}{680} = 2.06$ mA.
$P_{LED} = I_{Led} \times V_{Led} = 2.06mA \times 1.9V = 3.914mW$
$P_{R_{Led}} = I_{Led} \times V_{R_{Led}} = 2.06mW \times (3.3 - 1.9) = 2.884mW$
$P_{\text{LED-circuit}} = P_{R_{Led}} + P_{LED} = 6.8$ mW

R_{LED}= 680Ω	$P_{\text{LED-circuit}}$= 6.8 mW	/ 1 pt.

Q30: ESTIMATE THE POWER CONSUMPTION OF ONE INA201-BASED SENSING CIRCUIT

Calculate the maximum power consumption of the sensing circuit as $P_{\text{max,INA201}} = V_s \cdot I_{Q_{max}} + V_s \cdot I_{sc}$, where V_s is the supply voltage, $I_{Q_{max}}$ is the maximum quiescent current, and I_{sc} is short circuit output current corresponding to supply voltage. Carefully extract the values for $I_{Q_{max}}$ and I_{sc} from the datasheet based on your operating V_s to complete the calculation.

Added box
From datasheet : $I_{SC} = 15mA$, $I_{Q,max} = 1.6mA$
$P_{\text{INA201}} = 17mA \cdot 3.3V = 56$mW

$P_{\text{max,INA201}}$= 56 mW	/ 2 pt.

VOLTAGE MEASUREMENT

To sense the input and output DC voltage via the ADC of the digital controller, a voltage divider is used in this project. The voltage divider scales down the measured voltage, which is then filtered and buffered with an operational amplifier in voltage-follower configuration (i.e., unitary gain) before being connected to an ADC input of the DSP via the corresponding connector.
Fig.7 shows the typical circuit diagram of this voltage sensing circuit that will be used in this project. To protect the op-amp from over voltage, a diode is used between the position input and VCC. In this project, diode ES2C is used.

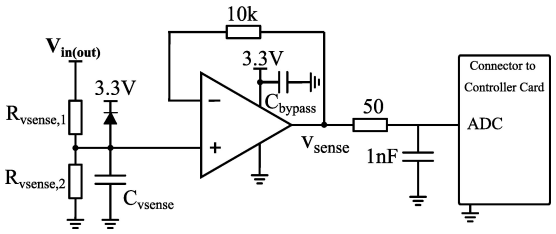


Figure 7 Typical DC voltage sensing circuit for the voltage $V_{in(out)}$.

Note: The operational amplifier MCP6241 is used to implement the voltage follower.

Q31: DESIGN THE VOLTAGE DIVIDER FOR INPUT VOLTAGE SENSING

Design the voltage divider in the voltage sensing circuit to ensure the voltage v_{sense} is below 3.0 V to respect the voltage limits of the downstream circuit. In doing this, a 10% margin should be kept on the maximum voltage. This constraint is described by the equation below.

$$1.1V_{max}\frac{R_{vsense,2}}{R_{vsense,1}+R_{vsense,2}} \leq 3.0V \tag{13}$$

In addition, it should be considered that the power dissipation on the resistor should not be too high. Moreover, the design of the low-pass filter can be realized by considering a target cut-off frequency of at least 1/10 of the switching frequency, calculated as

$$f_{cut-off} = \frac{1}{2\pi C_{vsense}(R_{vsense,1}//R_{vsense,2})} \tag{14}$$

Report the design for the primary voltage sensing (namely, the resistance and capacitance values selected from the Appendix, and the calculated power dissipation at maximum voltage) and the range of $v_{sense,pri}$ considering an input voltage from 0 to 60 V. And also considering the 12bit ADC of the used controller and the designed voltage divider, calculate the voltage sensing resolution. **Note: the cut-off frequency will determine the limit for the bandwidth of the control that will be implemented in the next report.**

From equation 13 and $V_{in,max} = 60\,V$ we get:

$$\frac{R_{vsense,2}}{R_{vsense,1}+R_{vsense,2}} \leq \frac{3.0\,V}{1.1\times 60\,V} = 0.04545$$

We select $R_{vsense,1,pri} = 97.6\,k\Omega$ (**KIT-RMCF1206FT-05**) and $R_{vsense,2,pri} = 4.64\,k\Omega$ (KIT-RMCF1206FT-04).
This leads to:

$$1.1\times 60\times\frac{4.64}{97.6+4.64} = 66\times\frac{4.64}{102.24} = 66\times 0.04538 = 2.995\,V \leq 3.0\,V \text{ (Verified)}$$

Power dissipation at $V_{in,max} = 60\,V$, with $I = 60\,V/102.24\,k\Omega = 0.587\,mA$:

$$P_{vsense,1,pri} = (0.587\,mA)^2\times 97.6\,k\Omega = 33.6\,mW \ll 250\,mW$$

$$P_{vsense,2,pri} = (0.587\,mA)^2\times 4.64\,k\Omega = 1.60\,mW \ll 250\,mW$$

For the low-pass filter, the parallel combination is:

$$R_{vsense,1}//R_{vsense,2} = \frac{97.6\times 4.64}{97.6+4.64} = \frac{452.9}{102.24} = 4.43\,k\Omega$$

We select $C_{vsense,pri} = 1\,nF$ (**C1206C102J1GACTU**, 100 V):

$$f_{cutoff} = \frac{1}{2\pi\times 1\,nF\times 4.43\,k\Omega} = 35.9\,kHz \geq \frac{f_{sw}}{10} = 25\,kHz$$

Sensing range for $V_{in} \in [0\,\text{V},\ 60\,\text{V}]$:

$$V_{sense,pri} = V_{in} \times \frac{R_{vsense,2}}{R_{vsense,1} + R_{vsense,2}} = V_{in} \times \frac{4.64}{102.24} \in [0\,\text{V},\ 2.72\,\text{V}]$$

Voltage sensing resolution (12-bit ADC, 0–3 V range):

$$V_{resolution,pri} = \frac{3\,\text{V}}{2^{12}} \times \frac{R_{vsense,1} + R_{vsense,2}}{R_{vsense,2}} = \frac{3}{4096} \times \frac{102.24}{4.64} = 16.1\,\text{mV per count}$$

$R_{\text{vsense,1,pri}}$= 97.6 kΩ | $P_{\text{vsense,1,pri}}$ = 33.6 mW | $R_{\text{vsense,2,pri}}$= 4.64 kΩ | $P_{\text{vsense,2,pri}}$ = 1.6 mW

$C_{\text{Vsense,pri}}$ = 1 nF | $V_{\text{sense,pri}}$: from 0 V to 2.72 V | $V_{\text{resolution,pri}}$: 16.1 $\times 10^{-3}$ V | / 3 pt.

Q32: DESIGN THE VOLTAGE DIVIDER FOR OUTPUT VOLTAGE SENSING

Similarly to the previous question, design the voltage divider for the output voltage sensing, and report the design values in the answer boxes. Additionally, report the $V_{\text{sense,sec}}$ corresponding to $V_{\text{out,rated}}$ in the answer box.

From equation 13 and $V_{out} = 24\,\text{V}$ we get:

$$\frac{R_{vsense,2,sec}}{R_{vsense,1,sec} + R_{vsense,2,sec}} \leq \frac{3.0\,\text{V}}{1.1 \times 24\,\text{V}} = 0.1136$$

We select $R_{vsense,1,sec} = 10\,\text{k}\Omega$ **RMCF1206FT10K0** and $R_{vsense,2,sec} = 1.21\,\text{k}\Omega$ (**KIT-RMCF1206FT-04**).
This leads to:

$$1.1 \times 24 \times \frac{1.21}{10 + 1.21} = 26.4 \times 0.1079 = 2.849\,\text{V} \leq 3.0\,\text{V (Verified)}$$

Power dissipation at $V_{out} = 24\,\text{V}$, with $I = 24\,\text{V}/11.21\,\text{k}\Omega = 2.14\,\text{mA}$:

$$P_{vsense,1,sec} = (2.14\,\text{mA})^2 \times 10\,\text{k}\Omega = 45.8\,\text{mW} \ll 250\,\text{mW}$$

$$P_{vsense,2,sec} = (2.14\,\text{mA})^2 \times 1.21\,\text{k}\Omega = 5.54\,\text{mW} \ll 250\,\text{mW}$$

For the low-pass filter:

$$R_{vsense,1,sec} // R_{vsense,2,sec} = \frac{10 \times 1.21}{10 + 1.21} = 1.079\,\text{k}\Omega$$

We select the same $C_{vsense,sec} = 1\,\text{nF}$ (**C1206C102J1GACTU**, 100 V):

$$f_{cutoff} = \frac{1}{2\pi \times 1\,\text{nF} \times 1.079\,\text{k}\Omega} = 147\,\text{kHz} \gg 25\,\text{kHz}$$

Sensing voltage at $V_{out,rated} = 24\,\text{V}$:

$$V_{sense,sec} = V_{out,rated} \times \frac{R_{vsense,2,sec}}{R_{vsense,1,sec} + R_{vsense,2,sec}} = 24 \times \frac{1.21}{11.21} = 2.59\,\text{V}$$

$R_{\text{vsense,1,sec}}$= 10 kΩ | $P_{\text{vsense,1,sec}}$ = 45.8 mW | $R_{\text{vsense,2,sec}}$= 1.21 kΩ | $P_{\text{vsense,2,sec}}$ = 5.54 mW

$C_{\text{Vsense,sec}}$ = 1 nF | $V_{\text{sense,sec}}$ = 2.59 V | / 3 pt.

Q33: ESTIMATE THE POWER CONSUMPTION FOR THE VOLTAGE FOLLOWER

The loss of the voltage follower circuit using the MCP6241 includes two parts: static power consumption and load power. In this application, the output of the circuit is connected to the digital isolation buffer (implemented in the controller board) by a connector, where the input impedance is high; thereby, the load current from the voltage follower is negligible, and therefore the load power can be neglected.

Refer to the note in Q30, estimate the power loss for the voltage follower circuit.

Added box

Since the load current is negligible (high-impedance input of the digital isolation buffer), only the static quiescent power needs to be estimated. From the **MCP6241 datasheet**, the typical quiescent supply current at $V_s = 3.3\,\text{V}$ is $I_Q = 100\,\mu\text{A}$:

$$P_{MCP6241,static} = V_s \times I_Q = 3.3\,\text{V} \times 100\,\mu\text{A} = 0.33\,\text{mW}$$

$P_{MCP6241,static}$ = 0.33 mW

/ 1 pt.

POWER SUPPLY FOR THE ICS

The gate driver, sensing circuit, and other ICs need a power supply to work. In this project, the ICs on the high-voltage input side are powered by the main input supply. The ICs on the output side are instead powered by the transformer's auxiliary winding. However, the voltage from the main input and transformer's auxiliary winding cannot be applied to the ICs directly because it needs to be regulated at the required value; therefore, voltage regulation circuits are needed.

Q34: ESTIMATE POWER CONSUMPTION OF 3.3V ON THE PRIMARY AND SECONDARY SIDE

The 3.3V power supply on the primary side needs to provide power for three INA201-based sensing circuits (one for DC input current and two for inductor current monitoring), one input voltage sensing circuit and two LED lighting circuits. Please calculate the overall power consumption of these circuits at the primary side.

As for the secondary side, the voltage regulation circuit needs to drive one voltage sensing circuit and one current sensing circuit. Please calculate the overall power consumption of these circuits at the secondary side.

Primary side (V_s = 3.3 V):

- Three INA201-based sensing circuits (1 DC input + 2 inductor monitoring): $3 \times P_{max,INA201} = 3 \times 56\,\text{mW} = 168\,\text{mW}$
- One input voltage sensing (MCP6241 follower): $P_{MCP6241} = 0.33\,\text{mW}$
- Two LED circuits (Q29): $2 \times 6.8\,\text{mW} = 13.6\,\text{mW}$

$$P_{pri,3.3V} = 168 + 0.33 + 13.6 = 182\,\text{mW}$$

Secondary side (V_s = 3.3 V):

- One output voltage sensing (MCP6241 follower): $P_{MCP6241} = 0.33\,\text{mW}$
- One DC output current sensing (INA201): $P_{max,INA201} = 56\,\text{mW}$

$$P_{sec,3.3V} = 0.33 + 56 = 56.3\,\text{mW}$$

$P_{pri,3.3V}$ = 182 mW	$P_{sec,3.3V}$ = 56.3 mW	/ 2 pt.

Q35: ESTIMATE LOAD CURRENT AND POWER CONSUMPTION OF 3.3V-LDO ON THE PRIMARY AND SECONDARY SIDE

To power the INA201 and operational amplifier with 3.3 V, two stage of DC-DC conversions are needed, one for the primary side and one for the secondary side. In this project, IC AZ1117IH-3.3TRG1 is asked to be used. The circuit for the use of AZ1117IH-3.3TRG1 is shown in Fig. 8. Here, one more LED is used. Combine the calculated power consumption on the 3.3V in the last question, calculate the load current of the 3.3V-LDO IC. And assuming power conversion efficiency of 60%, calculate the input power requirement for the 3.3V-LDO IC.

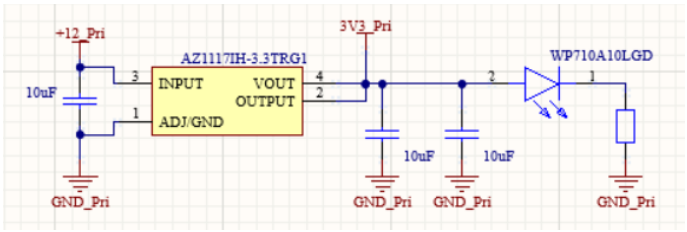


Figure 8 Example of the usage of the AZ1117IH-3.3TRG1 power conversion IC.

- **Primary side:**

$$I_{pri,3.3V} = \frac{P_{pri,3.3V}}{3.3V} + I_{Led} = \frac{182mW}{3.3V} + 2mA = 57mA$$

$$P_{pri,3.3V,in} = I_{pri,3.3V} \cdot \frac{3.3V}{0.6} = 312mW$$

- **Secondary side:**

$$I_{sec,3.3V} = \frac{P_{sec,3.3V}}{3.3V} + I_{Led} = \frac{56mW}{3.3V} + 2mA = 19mA$$

$$P_{sec,3.3V,in} = I_{sec,3.3V} \cdot \frac{3.3V}{0.6} = 104mW$$

$I_{pri,3.3V}$ = 57 mA	$I_{sec,3.3V}$ = 19 mA	$P_{pri,3.3V,in}$ = 312 mW	$P_{sec,3.3V,in}$ = 104 mW	/ 2 pt.

Q36: ESTIMATE POWER CONSUMPTION OF 12V ON THE PRIMARY AND SECONDARY SIDE

The 12V power supply on the primary side needs to provide power for two gate driver circuits, one 3.3V-LDO IC which convert 12V to 3.3V, and one LED circuit. Please calculate the overall power consumption and load current of 12V power supply at the primary side.

Similarly, the 12V power supply on the secondary side needs to provide power for two gate driver circuits, one LDO circuit which converter 12V to 3.3V, and one LED circuit. Please calculate the overall power consumption and load current of 12V power supply at the secondary side.
Note: In the practical design, the selected voltage regulation IC should provide stable 12V output, and out power and current capability should be higher than the calculated values and 50% margin should be considered.

One LED indicator (WP710A10LGD, $V_F \approx 1.9$ V) is used on each side at 12 V. We select **RMCF1206FT4K99** ($R_{LED} = 4.99\,\text{k}\Omega$):

$$I_{LED} = \frac{12 - 1.9}{4990} = 2.02\,\text{mA}, \qquad P_{LED,12V} = 12 \times 2.02\,\text{mA} = 24.3\,\text{mW}$$

Primary 12 V (2 gate drivers + 3.3 V LDO input + 1 LED):

$$P_{pri,12V} = 2 \times 67.6 + 312 + 24.3 = 471.5\,\text{mW}$$

$$I_{pri,12V} = \frac{471.5\,\text{mW}}{12\,\text{V}} = 39.3\,\text{mA}$$

Secondary 12 V (2 gate drivers + 3.3 V LDO input + 1 LED):

$$P_{sec,12V} = 2 \times 54.7 + 104 + 24.3 = 237.7\,\text{mW}$$

$$I_{sec,12V} = \frac{237.7\,\text{mW}}{12\,\text{V}} = 19.8\,\text{mA}$$

With the required 50% design margin, the regulation ICs must be rated for at least $1.5 \times 39.3 = 59$ mA (primary) and $1.5 \times 19.8 = 29.7$ mA (secondary).

$P_{pri,12V}$ = 471.5 mW	$I_{pri,12V}$ = 39.3 mA	$P_{sec,12V}$ = 237.7 mW	$I_{sec,12V}$ = 19.8 mA	/ 2 pt.

Q37: AUXILIARY POWER SUPPLY FOR THE ICS ON THE PRIMARY SIDE

On the primary side, the power for the auxiliary circuit is taken from the main input. To efficiently regulate the main input voltage (30V-60V) to a 12 V output for the auxiliary circuits, the DC-DC module 173951275 from Würth Elektronik is used in this project. The circuit for the use of 173951275 is shown in Fig. 10. To see if this power module works properly, a LED is used here (same as before, **LINK**). Calculate the LED current limiting resistor (resistance and power). Furthermore, to reduce output voltage ripple, select two appropriate capacitors from the Appendix based on the module's datasheet requirements.

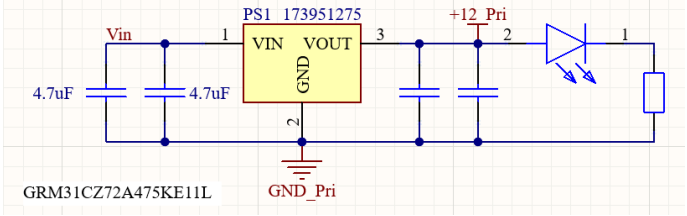


Figure 9 Example of the usage of the 173951275 power-conversion module.

Added box

The 173951275 module output is V_{out} = 12 V. Using the same LED (WP710A10LGD, $V_F \approx 1.9$ V, $I_{LED} \approx 2$ mA):

$$R_{LED,1} = \frac{12 - 1.9}{0.002} = 5050\ \Omega$$

We select **RMCF1206FT4K99** (4.99 kΩ, 1206). Actual current: (12 − 1.9)/4990 = 2.02 mA
Power dissipated in resistor:

$$P_{RLED,1} = (12 - 1.9) \times 2.02\ \text{mA} = 20.4\ \text{mW} \ll 250\ \text{mW}$$

Output capacitors: Following the **data sheet recommendations** , we choose two 22μF capacitors in parallel. We choose the **C5750X7S2A226M280KB** (22 μF, 100 V, X7S)

$R_{LED,1}$ = 4.99 kΩ	$P_{RLED,1}$ = 20.4 mW	$C_{out1,Pri,12V}$ = 22μ F	$C_{out2,Pri,12V}$ = 22μ F	/ 2 pt.

Q38: CALCULATE MINIMUM BLOCK VOLTAGE FOR THE DIODE RECTIFIER

To power the ICs on the secondary side, an extra winding is added to the transformer, which has been designed in Report 2. The voltage from the transformer cannot be applied to the ICs directly since it is AC voltage. Therefore, a diode rectifier is needed. In this project, the full-bridge rectifier, LMB14S-TP, is asked to be used.

Using the transformer's turns ratio get from report 2, calculate the repetitive peak reverse voltage (V_{RRM}) across the rectifier diodes when the system is stable at the rated output voltage.

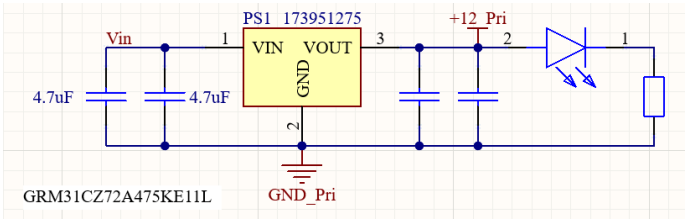


Figure 10 Example of the usage of the 173951275 power-conversion module.

Added box

Using the windings from Report 2, we get the peak voltage:

$$V_{aux,peak} = V_{in,max} \times \frac{N_{aux}}{N_{pri}} = 60 \times \frac{8}{21} \approx 22.86\ \text{V}$$

Each diode in the full-bridge rectifier (LMB14S-TP) must block the full peak voltage when reverse-biased:

$$V_{RRM} = V_{aux,peak} = 22.86\ \text{V}$$

The LMB14S-TP is rated V_{RRM} = 400 V ≫ 22.86 V

V_{RRM} = 22.86 V	/ 1 pt.

Q39: SELECTION OF CAPACITANCE FOR THE DIODE RECTIFIER CIRCUIT

To obtain a stable DC voltage after the rectifier, capacitors are needed. Assuming the voltage ripple is 1% and the load current, $I_{load,aux}$, is 0.3 A for this auxiliary circuit, calculate the filter capacitor and find the closest standard value. To protect the follower LDO IC from over voltage damage, a zener diode, 1N4750A-TR, is placed in parallel with the output.
The minimal capacitance can be calculated by

$$C_{min} = \frac{I_{load,aux}}{2 \cdot f_{sw} \cdot V_{ripple}} \tag{15}$$

The allowed voltage ripple is 1%:

$$V_{ripple} = 1\% \cdot V_{\text{RRM}} = 0.01 \times 22.87 = 0.2287\,\text{V}$$

The minimum filter capacitance with $I_{load,aux} = 0.3$ A and $f_{sw} = 250$ kHz:

$$C_{min} = \frac{I_{load,aux}}{2 \cdot f_{sw} \cdot V_{ripple}} = \frac{0.3}{2 \times 250 \times 10^3 \times 0.2287} = 2.62\,\mu\text{F}$$

We choose the GRM31CZ72A475KE1 (4.7 μF, 100 V, X7R, 1206).

$C_{rectifier(min)}$ = 2.62 μ F	$C_{rectifier(select)}$ = 4.7 μ F	$V_{rated-C}$ = 100 V	/ 1 pt.

Q40: CALCULATE THE LOAD CURRENT FOR LDO-12V ON THE SECONDARY SIDE

On the secondary side, to regulate the output from the rectifier to 12V to power the secondary-side gate drivers, an extra LDO is needed. In this project course, the UA78L12ACDR is suggested. Refer to section 8.2 of the datasheet (LINK), select the input and output capacitors. And check if the current capability of this IC is higher than the calculated load current on the 12-V on the secondary side.

From the data sheet: *"Although not required, a 0.33-µF bypass capacitor is recommended on the input, and a 0.1-µF bypass capacitor is recommend on the output."*
We choose the **C1206C334K5RACTU** (0.33 μF, 50 V, X7R) as $C_{\text{LDO-12V,in}}$ and **C1206C104K5RACTU** (0.1 μF, 50 V, X7R) as $C_{\text{LDO-12V,out}}$.
We also get that $I_{out,max}$ = 100mA. From Q36, $I_{\text{sec,12V}}$ = 19.8 mA $\ll$ 100mA.

$C_{\text{LDO-12V,in}}$ = 0.33 μF	$C_{\text{LDO-12V,out}}$ = 0.1 μF	/ 1 pt.

SCHEMATIC AND PCB

In this project, main input and output connector will be provided in the template. Below connector with a specific pin map should be used, which is the interface between the power board and controller. The connector will be provided in the Alitum Designer Template. PWM channel 1 and channel 2 should be used for the primary side; PWM channel 3 and channel 4 should be used for the secondary side; ADC A0 and A1 is used for output voltage and output current sensing. ADC A2 and A3 is used for input voltage and input current sensing. $ECAP2_{ISO}$ is for inductor current over current detection circuit. $GPIO15_{ISO}$ is connected to a red LED; $CS1_{ISO}$, and $CS2_{ISO}$ are connected to two green LEDs. To limit the current of 2mA, resistor is needed.

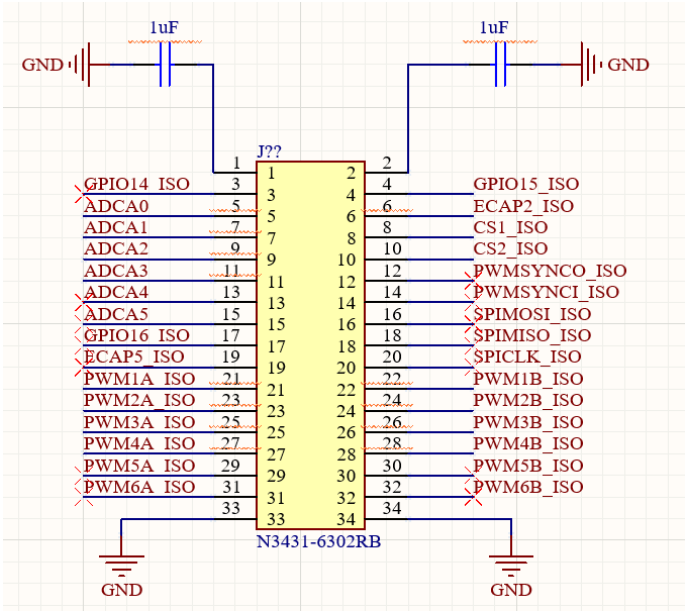
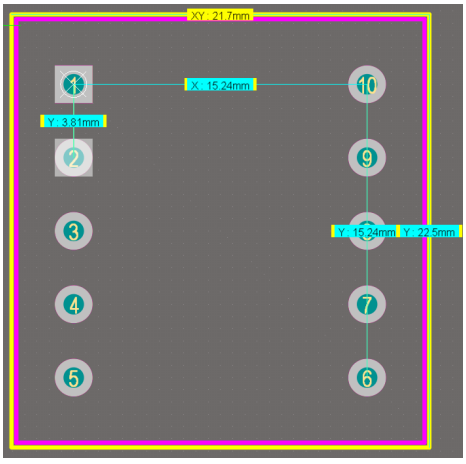


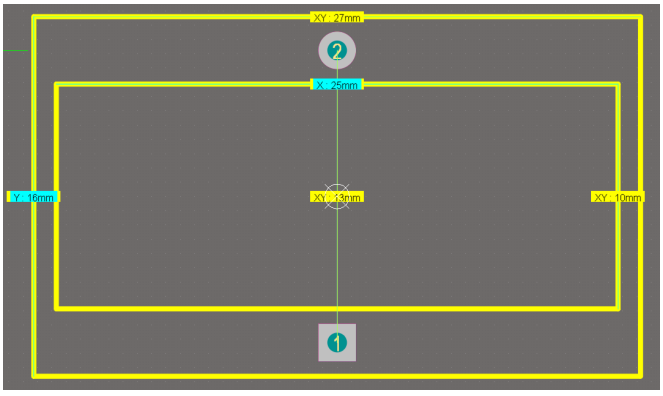
Figure 11 Interfacing connector between the power board and control board.

Q41: CREATE THE FOOTPRINTS

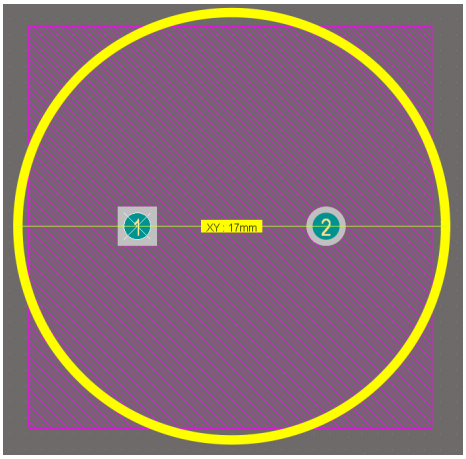
Please design the footprints for the transformer, inductor, and input electrolytic capacitor, and then report the figures of the footprint in the framed box. Use the measurement tool to show the relevant geometric dimensions of the footprint as in the exemplary figure below.



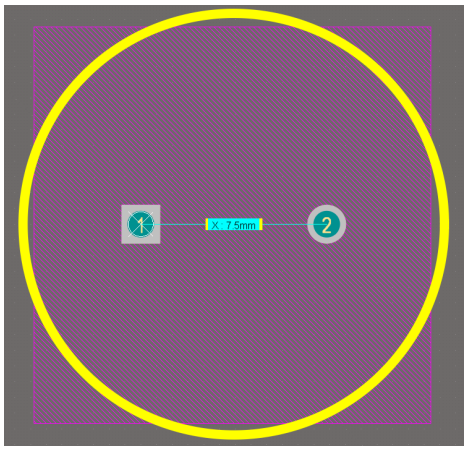
Footprint of the transformer



Footprint of the inductor



Footprint of the electrolytic capacitor (diameter)



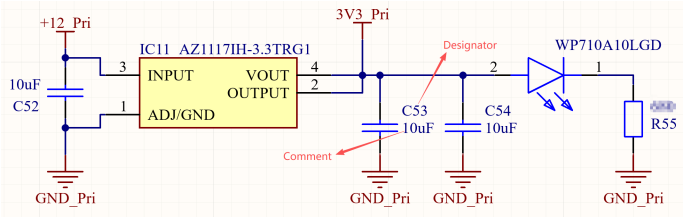
Footprint of the electrolytic capacitor (Pin distance)

/ 6 pt.

Q42: SCHEMATIC LAYOUT

Follow the instructions below to finalize your Altium Designer schematic. Once complete, export the schematic as a PDF for TA review.

- Finish the connection between the components; include capacitance and resistance values in the parameters/comments, as shown in below figure.



- Place test points in the schematic. The provided model of test point has two connection terminals, which must be connected to the desired signal and to the corresponding ground. Place Test-Points to measure the following signals:
  - The drain-source voltage of all low-side devices.
  - The gate-source voltage of all low-side devices.
  - The voltage across the three shunt resistors.
  - All PWM signals from the digital controller.
  - 12V and 3.3V on the both primary and secondary side.
  - Auxiliary voltage (V_{aux}).
  - Output of the inductor current monitoring circuit.
  - Output of the voltage and current measurement circuit.
- Place the heatsinks for the MOSFETs. Choose the correct footprints, coherently with the models chosen in report 1. Leave their mounting connection terminals floating.
- Place 4 M3 mounting holes.

/ 5 pt.

Q43: BILL OF MATERIALS (BOM)

With the help of the Altium Report Manager, generate the Bill of Materials (BOM) needed to build your converter and include it below. This report-type document provides a list of all the required components for design realization.

In case your design requires the use of additional components not listed in the Appendix section, highlight them and be sure to provide the following information in tabular form:
• Manufacturer Part Number;
• Supplier Part Number (e.g., Digikey, Mouser, etc...);
• Supplier Link;
• Quantity (n.b., check that the needed quantity is available in stock, and that it is possible to order the exact amount needed);
• Unit Price (in CHF);

• Total Price (in CHF).

Refer, if possible, to a single supplier for all your additional required components. The Appendix provides some constraints for the additional components that can be allowed in your design.

Our design does not use any additional component than the given ones. Below is the list of material, providing that some were unavailable. The standard resistors and capacitor were omitted (included in the appendix).

Value/Name	Description	Footprint	Mouser Number	Qty	Price (CHF)
–	Connector 2 pos	PHOENIX 1755736	651-1755736	2	0.444
0.01u	Capacitor (non polarized)	SM/1206	–	2	–
0.1u	Capacitor (non polarized)	SM/1206	–	3	–
0.33u	Capacitor (non polarized)	SM/1206	–	1	–
1n	Capacitor (non polarized)	SM/1206	–	6	–
1N4750A-TR	Zener Diode	DIOAD1310W86L370D235	78-1N4750A	1	0.325
1u	Capacitor (non polarized)	SM/1206	–	4	–
1uF	Capacitor (non polarized)	SM/1206	–	2	–
1.21k	Resistor (Surface Mounted)	SM/1206	–	1	–
1.65k	Resistor (Surface Mounted)	SM/1206	–	8	–
1.88 u	Capacitor (non polarized)	SM/1206	–	2	–
2.2k	Resistor (Surface Mounted)	SM/1206	–	2	–
4.64k	Resistor (Surface Mounted)	SM/1206	–	1	–
4.7 u	Capacitor (non polarized)	SM/1206	–	3	–
4.7u	Capacitor (non polarized)	SM/1206	–	3	–
4.99	Resistor (Surface Mounted)	SM/1206	–	4	–
4.99k	Resistor (Surface Mounted)	SM/1206	–	1	–
10	Resistor (Surface Mounted)	SM/1206	–	8	–
10k	Resistor (Surface Mounted)	SM/1206	–	14	–
10k	Variable Resistor	TRIMMER CT-6EP	229-CT-6EP103	2	0.738
10m	Shunt Resistor	CSNL2512FT5L00	–	1	–
10p	Capacitor (non polarized)	SM/1206	–	8	–
10u	Capacitor (non polarized)	SM/1206	–	6	–
20m	Shunt Resistor	CSNL2512FT5L00	–	1	–
22 u	Capacitor (non polarized)	SM/2220	–	1	–
22u	Capacitor (non polarized)	SM/1206	–	2	–
25m	Shunt Resistor	CSNL2512FT5L00	–	1	–
25.5k	Resistor (Surface Mounted)	SM/1206	–	2	–
28.7 k	Resistor (Surface Mounted)	SM/1206	–	1	–
50	Resistor (Surface Mounted)	SM/1206	–	4	–
51.1	Resistor (Surface Mounted)	SM/1206	–	6	–
68n	Capacitor (non polarized)	SM/1206	–	7	–
97.6k	Resistor (Surface Mounted)	SM/1206	–	1	–
200k	Resistor (Surface Mounted)	SM/1206	–	1	–
680	Resistor (Surface Mounted)	SM/1206	–	7	–
680 u	Capacitor	Electrolytic (UHW2A681MHD)	647-UHW2A681MHD	1	2.880
173951275	Power Supply	173951275	710-173951275	1	4.400
AZ1117IH-3.3TRG1	Integrated Circuit	SOT230P700X180-4N	621-AZ1117IH-3.3TRG1	2	0.190
ES2C	Schottky Diode	DIOM5436X244N	not found	8	–
Heatsink	Heatsink TO-218/220/247	Heatsink EA-T220-38E	588-EA-T220-38E	4	unavailable
INA201AID	Integrated Circuit	SOIC127P600X175-8N	595-INA201AIDR	4	3.600
Inductor	Custom (T94-2)	Custom footprint	–	1	–
LMB14S-TP	Full-bridge rectifier	LMB14STP	833-LMB14S-TP	1	0.357
MCP6241-E/P	Integrated Circuit – Op Amp	DIP781W56P254L950H533Q8N	579-MCP6241-E/P	2	0.341
MOSFET	N-Channel Power MOSFET	TO-220AB	1727-PHP18NQ11T (digikey)	8	2.300
N3431-6302RB	Connector	3M N3431-6302RB	517-N3431-6302RB	1	3.940
Test point	Test point	Test Point	200-TSW20207TS	3	0.198
TL3305BF100QG	Push Button	TL3305BF160QG	612-TL3305BF100QG	1	0.167
Transformer	Custom (B66206B1110T001)	Custom footprint	–	1	–
UA78L12ACDR	Integrated Circuit	SOIC127P600X175-8N	595-UA78L12ACDR	1	0.293
UCC27288DR	Integrated Circuit	SOIC127P600X175-8N	595-UCC27288DR	4	1.390
WP710A10LGD	LED Green	WP710A10LGD	604-WP710A10LGD	7	0.174
WP710A10LID	LED Red	WP710A10LID	604-WP710A10LID	1	0.198
				Total	**56.16**

Table 3 Bill of Materials (BOM) for the DAB converter PCB.

/ 2 pt.

Q44: MINIMAL COPPER WIDTH FOR CURRENT-CARRYING TRACKS

Prior to routing your PCB, determine the minimal copper width needed for the current-carrying tracks. The copper thickness is fixed to 35 μm(1 OZ), whereas the current density is limited to 35 A/mm^2, to limit the copper temperature rise to roughly 10 degrees. Based on this information and the rated current, calculate your current-carrying track width and proceed with it for the power stage.
Note: it is clear that this width must be applied only to the connections that carry high current, not to every trace in the PCB.

The minimal copper track width is determined by the current density limit $J = 35\,\text{A/mm}^2$ and copper thickness $t = 35\,\mu\text{m} = 0.035\,\text{mm}$:

$$w = \frac{I_{\text{rms}}}{J \cdot t}$$

Primary side: the limiting current is the inductor RMS current, derived from the worst-case PLECS simulation of Report 1 ($I_{Q,pri,rms} = 1.47\,\text{A}$ per MOSFET, half-wave):

$$I_{L,rms} = \sqrt{2} \times I_{Q,pri,rms} = \sqrt{2} \times 1.47 = 2.08\,\text{A}$$

$$w_{\text{cu,pri}} = \frac{I_{L,rms}}{J \cdot t} = \frac{2.08}{35 \times 0.035} = \frac{2.08}{1.225} = 1.70\,\text{mm}$$

Secondary side: from the worst-case PLECS simulation of Report 1 : $I_{Q,sec,rms} = 3.06\,\text{A}$.

$$w_{\text{cu,sec}} = \frac{I_{Q,sec,rms}}{J \cdot t} = \frac{3.06}{35 \times 0.035} = \frac{3.06}{1.225} = 2.50\,\text{mm}$$

These widths apply only to high-current power-stage traces (H-bridge loops, shunt resistor connections, input/output bus).

$w_{\text{cu,pri}} = 1.70$ mm | $w_{\text{cu,sec}} = 2.50$ mm

/ 2 pt.

Q45: PCB LAYOUT

Before manufacturing the PCB of the designed converter, it is necessary to check that the connections and component placement were done correctly. For this purpose, route your PCB, following the guidelines given below.
For this course, the PCB prototype is limited to 2 layers. It is not allowed to exceed the maximum size set by the provided template.
For best performance, partition the PCB by physically grouping components:

- Power circuitry (MOSFET, inductor, input and output capacitors, input and output terminals, etc...);
- Gate driving circuit.

Looking into **Link**. This guide is a technical resource for the entire design process, which covers the essential rules for schematics, layout, and manufacturing that every engineer and hobbyist needs to know for a successful design.
The rules for PCB layout has been set in the Altium Template. Auto-routing is not allowed.
Route in the following order:

- Power stage (MOSFET, diode, coupled inductor...) to have the minimum physical loop on the board, as this loop will be the source of interference.
- Auxiliary measurement and control circuits. To avoid problems that are difficult to solve later, it is strongly suggested to follow closely the layout guidelines provided in the datasheet of the integrated circuits.

You can use vias to connect tracks on the two sides of the PCB.

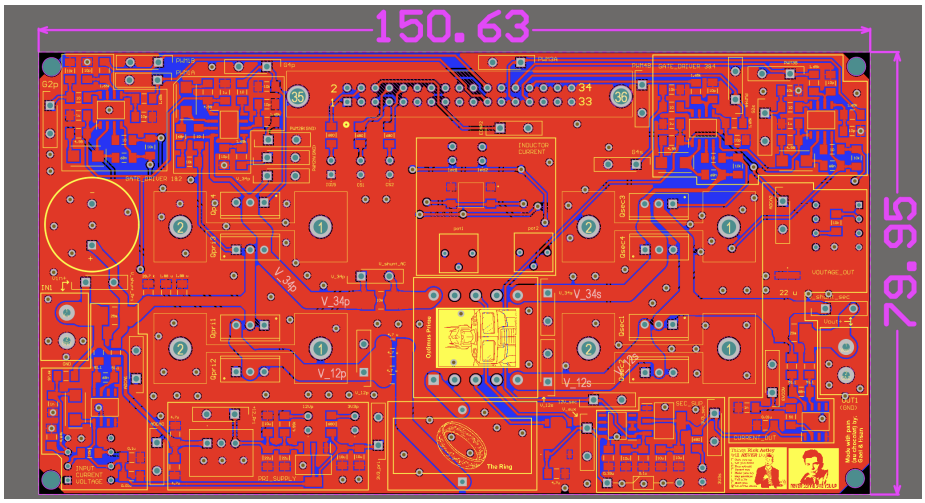
Place the mounting holes near the corners of the board to ensure good mechanical stability.

Verify that the heatsinks are properly aligned with the MOSFETs.

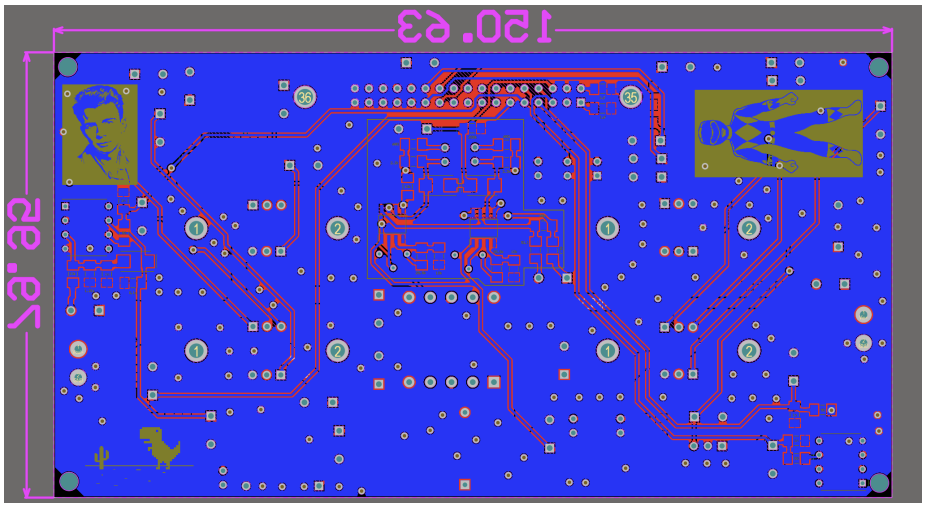
Annotate the PCB silkscreen with all the required information (e.g., connector polarities, component identifiers, etc...).

Run a design rule check in Altium Designer, and correct all the errors.

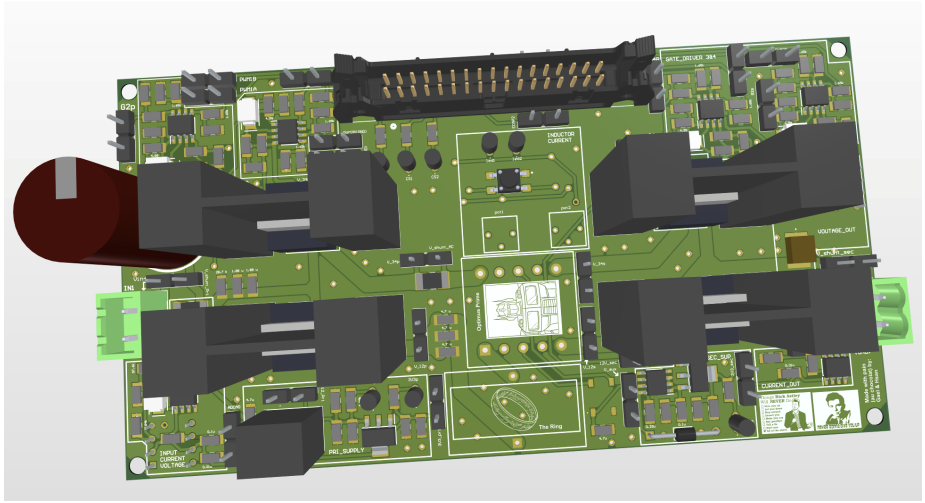
Include below a 2D and 3D view of the top and bottom layers of your final PCB layout.



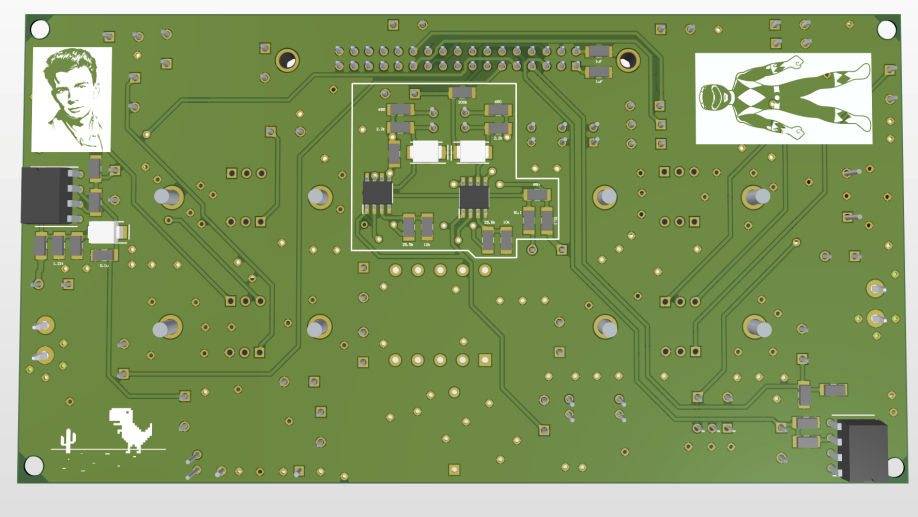
Top layer



Bottom layer



Top layer (3D)



Bottom layer (3D)

/ 5 pt.

APPENDIX

This section contains the list of available components that can be used in your design, and some specification requirements for additional components.

LIST OF AVAILABLE SMD CAPACITORS

The list of available SMD Ceramic Capacitors is given in Table 5. Refer to these values for your design.
For information about the power ratings of different SMD ceramic capacitors, refer to Table 4.

Table 4 Power ratings of different SMD ceramic capacitors packages, empirically determined considering a temperature rise of 25 °C rise above the ambient temperature (Source: Johanson Dielectrics).

Package (Imperial/Metric)	1206/3216	1210/3225	1812/4532	2512/6332
Power Rating	80 mW	200 mW	400 mW	900 mW

Table 5 List of available SMD Ceramic Capacitors

Manufacturer	Part Number	Package (Imperial/Metric)	Capacitance		Tolerance (%)	Rated Voltage (V)
KEMET	C1206C100J2GACTU	1206/3216	10	pF	±5	200
KEMET	C1206C220F2GACTU	1206/3216	22	pF	±1	200
KEMET	C1206C330F2GACTU	1206/3216	33	pF	±1	200
KEMET	C1206C470F2GACTU	1206/3216	47	pF	±1	200
KEMET	C1206C101J1GACTU	1206/3216	100	pF	±5	100
KEMET	C1206C221J1GACTU	1206/3216	220	pF	±5	100
KEMET	C1206C471J1GACTU	1206/3216	470	pF	±5	100
KEMET	C1206C102J1GACTU	1206/3216	1000	pF	±5	100
KEMET	C1206C222K1GACTU	1206/3216	2200	pF	±10	100
KEMET	C1206C472K5GACTU	1206/3216	4700	pF	±10	50
KEMET	C1206C222K2RACTU	1206/3216	2200	pF	±10	200
KEMET	C1206C104K5RACTU	1206/3216	0.1	µF	±10	50
KEMET	C1206C154K5RACTU	1206/3216	0.15	µF	±10	50
KEMET	C1206C224K5RACTU	1206/3216	0.22	µF	±10	50
KEMET	C1206C334K5RACTU	1206/3216	0.33	µF	±10	50
KEMET	C1206C474K3RACTU	1206/3216	0.47	µF	±10	25
KEMET	C1206C105K3RACTU	1206/3216	1	µF	±10	25
KEMET	C1206C225K5RACTU	1206/3216	2.2	µF	±10	50
KEMET	C1206C106K4RACTU	1206/3216	10	µF	±10	16
KEMET	C1206C225K4PACTU	1206/3216	2.2	µF	±10	16
KEMET	C1206C335K3PACTU	1206/3216	3.3	µF	±10	25
KEMET	C1206C475K3PACTU	1206/3216	4.7	µF	±10	25
KEMET	C1206C106K4PACTU	1206/3216	10	µF	±10	16
KEMET	C1206C226M4PACTU	1206/3216	22	µF	±20	16
KEMET	C1206C472J5GECTU	1206/3216	4.7	nF	±5	50
KEMET	C1206C103J5RAC	1206/3216	10	nF	±5	50
KEMET	C1206C223J5RACAUTO	1206/3216	22	nF	±5	50
KEMET	C1206C273J5RACTU	1206/3216	27	nF	±5	50
KEMET	C1206C683J1RECAUTO	1206/3216	68	nF	±5	100
Murata	GRM31CZ72A475KE1	1206/3216	4.7	uF	±10	100
TDK	C5750X7S2A226M280KB	2220/5750	22	uF	±20	100
TDK	CGA5L1X7R1H106K160AC	1206/3216	10	uF	±10	50
Vishay	MAL215097614E3	Create footprint by your own	1000	uF	±20	25

LIST OF AVAILABLE SMD RESISTORS

The SMD Resistors can be chosen from Table 7. This table includes both SMD resistor kits and individual resistor values.
For the resistance codes of the Stackpole Electronics Kits it is possible to refer to Fig.12.

Table 6 List of available SMD Resistors (Individual and Kits).

Manufacturer	Part Number	Package (Imperial/Metric)	Resistance Value(s) (Single or Kit)	Tolerance (%)	Rated Power (W)
Stackpole Electronics	KIT-RMCF1206FT-02	1206/3216	**E96 values** from 10 Ω to 97.6 Ω	±1	0.25
Stackpole Electronics	KIT-RMCF1206FT-03	1206/3216	**E96 values** from 100 Ω to 976 Ω	±1	0.25
Stackpole Electronics	KIT-RMCF1206FT-04	1206/3216	**E96 values** from 1 kΩ to 9.76 kΩ	±1	0.25
Stackpole Electronics	KIT-RMCF1206FT-05	1206/3216	**E96 values** from 10 kΩ to 97.6 kΩ	±1	0.25
Stackpole Electronics	RMCF1206FT2R00	1206/3216	2 Ω	±1	0.25
Stackpole Electronics	RMCF1206FT4R99	1206/3216	4.99 Ω	±1	0.25
Stackpole Electronics	RMCF1206FT10R0	1206/3216	10 Ω	±1	0.25
Stackpole Electronics	RMCF1206FT100R	1206/3216	100 Ω	±1	0.25
Stackpole Electronics	RMCF1206FT680R	1206/3216	680 Ω	±1	0.25
Stackpole Electronics	RMCF1206FT4K99	1206/3216	4.99K Ω	±1	0.25
Stackpole Electronics	RMCF1206FT10K0	1206/3216	10K Ω	±1	0.25

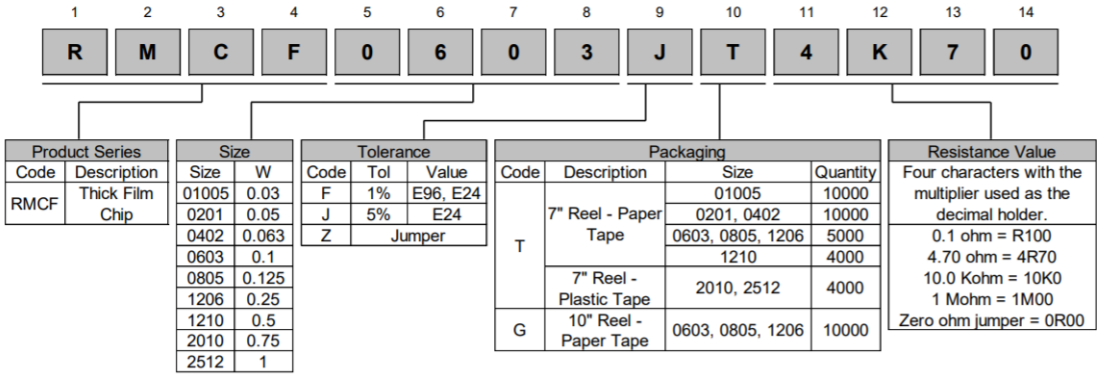


Figure 12 Resistor Code for Stackpole Electronics Kits.

LIST OF AVAILABLE SHUNT RESISTORS

Table 7 List of available SMD Current-Shunt Resistors.

Manufacturer	Part Number	Package (Imperial/Metric)	Resistance Value (%)	Tolerance Power (W)	Rated	Temperature Coefficient
SEI Stackpole	CSNL2512FT3L00	2512/6432	3 mΩ	1%	2 W	50 PPM / C
SEI Stackpole	CSNL2512FT4L00	2512/6432	4 mΩ	1%	2 W	50 PPM / C
SEI Stackpole	CSNL2512FT5L00	2512/6432	4 mΩ	1%	2 W	50 PPM / C
SEI Stackpole	CSNL2512FT7L00	2512/6432	7 mΩ	1%	2 W	50 PPM / C
SEI Stackpole	CSNL2512FT10L0	2512/6432	10 mΩ	1%	2 W	50 PPM / C
SEI Stackpole	CSNL2512FT15L0	2512/6432	15 mΩ	1%	3 W	50 PPM / C
SEI Stackpole	CSNL2512FT20L0	2512/6432	20 mΩ	1%	3 W	50 PPM / C
SEI Stackpole	CSNL2512FT25L0	2512/6432	25 mΩ	1%	3 W	50 PPM / C
SEI Stackpole	CSNL2512FT30L0	2512/6432	30 mΩ	1%	3 W	50 PPM / C
SEI Stackpole	CSNL2512FT39L0	2512/6432	39 mΩ	1%	3 W	50 PPM / C
SEI Stackpole	CSNL2512FT50L0	2512/6432	50 mΩ	1%	3 W	50 PPM / C

RULES FOR ADDITIONAL COMPONENTS

Only the following components can be authorized:

- Input and Output capacitors;
- Auxiliary circuit Limiting Resistor;
- Gate Resistor.

Note also that: Additional **SMD** components are limited to the package **1206 or bigger**;
To this purpose, the group is asked to provide in Q43 the following information in tabular form:

- Manufacturer Part Number;
- Supplier Part Number (e.g., Digikey, Mouser, etc...);
- Supplier Link;
- Quantity (n.b., check that the needed quantity is available in stock, and that it is possible to order the exact amount needed);
- Unit Price (in CHF);
- Total Price (in CHF).

Refer, if possible, to a single supplier for all your additional required components.