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Title

R1: DAB CONVERTER – BASIC DESIGN AND SIMULATIONS

Course Name

EE-365 Power Electronics

Keywords

DAB Converter, PLECS, Design, Modelling, Simulations

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DAB CONVERTER SIZING

The first part of the project deals with the basic design calculations and sizing the main elements of a DC-DC DAB converter, according to the given converter specifications and design requirements. **Fill out** Table 1 with the parameters assigned to your group, and do not forget to add your names in the report's header. Regarding the results of analytical calculations, please provide them rounded to two digits after the decimal point in the units provided in the solution box. Use the framed boxes below each question to insert your answers and explanations. Keep them concise.

Table 1 Design parameters and requirements for the DAB converter.

Property	Value	Unit
$P_{out,nom}$	50	W
$U_{in,nom}$	50	V
$U_{in,min}$	30	V
$U_{in,max}$	60	V
U_{out}	24	V
$\Delta U_{out,pp,rel}$	2	%
f_{sw}	250	kHz

Q1: TRANSFORMER TURN RATIO

The best value of the turn ratio of transformer n is $\frac{V_{pri}}{V_{sec}}$
Design the transformer turns ratio to ensure that you can obtain the desired output voltage when working at $V_{in,nom}$.

$$n = \frac{V_{pri}}{V_{sec}} = \frac{50}{24} = \frac{25}{12} = 2.0833$$

$n = \frac{25}{12} = 2.08$ / 2 pt.

Q2: INDUCTOR L

NOTE: You may have to iterate between Q2 and Q3 in case of the L value doesn't satisfy the converter requirements.

The power transfer relation of the DAB converter is given by Equation 1

$$P = \frac{nV_{pri}V_{sec}\varphi(\pi - |\varphi|)}{2\pi^2 f_{sw}L} \tag{1}$$

where n is the transformer turn ratio, V_{pri} is the primary side voltage, V_{sec} is the secondary side voltage, φ is the phase shift in radians, f_{sw} is the switching frequency, and L is the relevant DAB inductance.
Adding significant safety margin above the nominal power, the maximum power is designed to be **twice (correction : 3 times)** the rated power. Please indicate at which φ_{Pmax} the maximum power transfer occurs, and then calculate the corresponding inductance L for an operation at nominal input and output voltages.

P_{max} is obtain when $\varphi(\pi - |\varphi|)$ is maximum. This occurs at $\pi/2$, so $\varphi_{Pmax} = \frac{\pi}{2}$ then $\varphi_{Pmax}(\pi - |\varphi_{Pmax}|) = \frac{\pi^2}{4}$
The corresponding inductance can then be isolated from $P = \frac{nV_{pri}V_{sec}\varphi(\pi-|\varphi|)}{2\pi^2 f_{sw}L}$:

$$L = \frac{nV_{pri}V_{sec}\varphi_{Pmax}(\pi - |\varphi_{Pmax}|)}{2\pi^2 f_{sw}P_{max}} = \frac{nV_{pri}V_{sec}\pi^2}{4 \times 2\pi^2 f_{sw} \cdot 3P_{out,norm}} = \frac{nV_{pri}V_{sec}}{24 f_{sw}P_{out,norm}} = 8.33 \times 10^{-6} \text{ H}$$

$\varphi_{Pmax} = \frac{\pi}{2}$ rad $L = 8.33 \times 10^{-6}$ H / 4 pt.

Q3: VERIFY L WITH MINIMAL INPUT VOLTAGE

The DAB converter must be able to deliver nominal power for its entire range of operation, here, namely, for all input voltages.

Using Equation 1, draw a curve of the relationship between the input voltages and the maximum transferred power.

NOTE: The input voltage varies between 30 V and 60 V, resulting in different maximum powers.

Now, check the maximum output power curve. When the input voltage is at its minimum value, can the converter still output its rated power? If not, re-size the inductor L for higher transfer power, and derive a final value of L.

For the whole range of values $V_{sec} \in [30\ V\ ;\ 60\ V\ ;\ ]$ the output power stays greater than the nominal power of 50 W meaning that the the converter is able to output a power greater than its rated power even for the minimal input voltage. Thus, we do not have to resize the inductance.

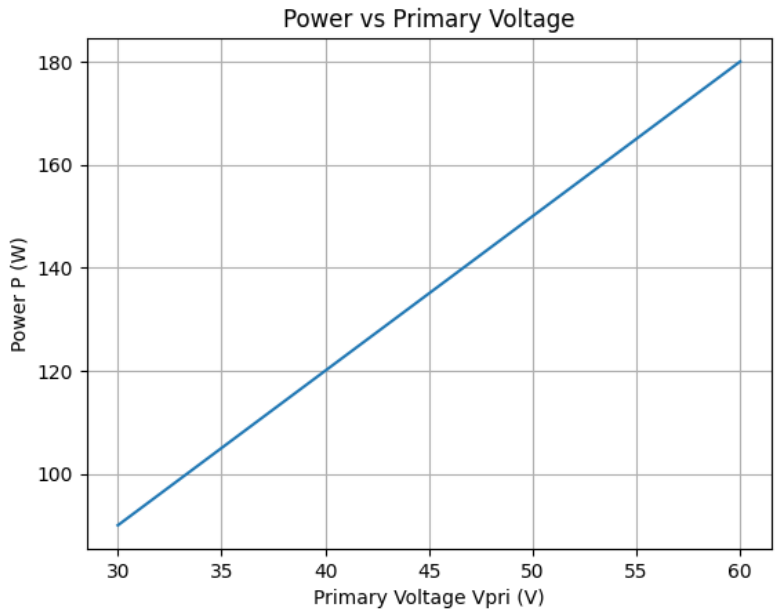


Figure 1 The relationship between the maximum power and the input voltage.

$L = 8.33 \times 10^{-6}$ H

/ 4 pt.

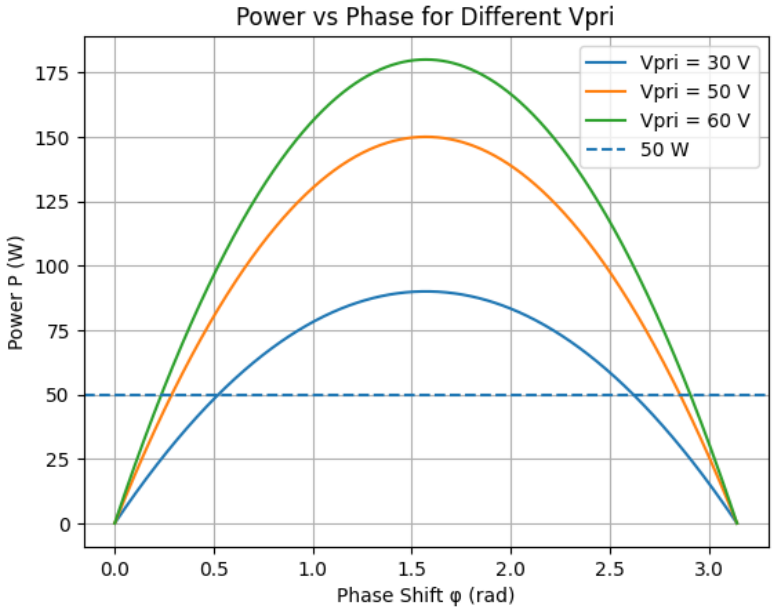
Q4: RANGE OF THE PHASE SHIFT, Φ

Calculate the phase shift by Equation 1. When you have minimum, maximum, and nominal input voltages, what are the corresponding phase shifts φ_{Vmin}, φ_{Vmax}, and φ_{Vnom} to achieve nominal power?

From the equation : $P = \frac{nV_{pri}V_{sec}\varphi(\pi - |\varphi|)}{2\pi^2 f_{sw}L}$, we see that $\varphi > 0$ and can isolate :

$$\varphi(\pi - \varphi) = \frac{2.P.\pi^2 f_{sw}.L}{n.V_{pri}.V_{sec}} \quad ; \quad P = P_{out,nom} = 50\text{W} \text{ and } V_{pri} \in \{30, 50, 60\}\text{V}$$

Graphicaly, this gives us :



V_{min} = 30 V -> φ_{Vmin} = 0.524 rad (or 2.618 rad)
V_{max} = 60 V -> φ_{Vmax} = 0.236 rad (or 2.906 rad)
V_{nom} = 50 V -> φ_{Vnom} = 0.288 rad (or 2.853 rad)

φ_{Vmin} = 0.52 rad	φ_{Vmax} = 0.24 rad	φ_{Vnom} = 0.29 rad	/ 3 pt.

Q5: OUTPUT CAPACITANCE, C_{OUT}

NOTE: Take into account the worst operating condition. Calculate with the following steps:

1. Calculate the output DC current I_{out} at nominal power
2. Calculate currents I_1 and I_2 as defined in the course's slides at the nominal power and lowest input voltage
3. Draw and plot the current waveform of the inductor i_L for one period
4. Draw and plot the current waveform of the output current of secondary side full bridge $i_{FB,out}$ for one period
5. Draw and plot the current waveform $\Delta i = i_{FB,out} - I_{out}$ for one period
6. Based on this curve, calculate the ripple charge of the output capacitor ΔQ (i.e., the charge that causes the output voltage ripple)
7. Calculate C_{out}

1) At the nominal power : $P = 50W$, $V_{out} = 24V \Rightarrow I_{out} = \frac{P}{V_{out}} = \frac{25}{12} = 2.083$ A

2) Since we are considering the case of the nominal power $P_{out} = 50$W and lowest input voltage $U_{in,min} = 30$V (with a duty cycle of 0.5), the currents at the switching transitions are calculated using the phase shift $\varphi_{Vmin} = 0.524$ rad, minimum input voltage $V_p = 30$ V, and reflected secondary voltage $|nV_s| = 50$ V:

$I_1 = \frac{T_s}{4L}\left(|nV_s| + V_p\frac{2\varphi-\pi}{\pi}\right) = \frac{4\times10^{-6}}{4\times8.33\times10^{-6}}\left(50 + 30\frac{2(0.524)-\pi}{\pi}\right) = 3.60$ A

$I_2 = \frac{T_s}{4L}\left(V_p + |nV_s|\frac{2\varphi-\pi}{\pi}\right) = \frac{4\times10^{-6}}{4\times8.33\times10^{-6}}\left(30 + 50\frac{2(0.524)-\pi}{\pi}\right) = -0.40$ A

3) 4) 5) See the figure below.

6) The peak current flowing into the output capacitor occurs right after the secondary side switches, generating a peak $\Delta i = nI_1 - I_{out} = 2.0833 \times 3.60 - 2.083 = 5.42$ A. The slope can be found from y $n.v_L/L = n(V_p - nV_s)/L = -5.00$ A/μs.
The time to reach zero current at the capacitor ($i_{FB,out} = I_{out}$) is 5.42/5.00 = 1.08 μs.
Integrating this positive triangular area gives the ripple charge: $\Delta Q = \frac{1}{2} \times 5.42 \times 1.08 \times 10^{-6} = 2.94 \times 10^{-6}$ C.

7) For a 2% voltage ripple ($\Delta U_{out,pp} = 0.48$ V): $C_{out} = \frac{\Delta Q}{\Delta U_{out,pp}} = \frac{2.94\times10^{-6}}{0.48} = 6.12 \times 10^{-6}$ F

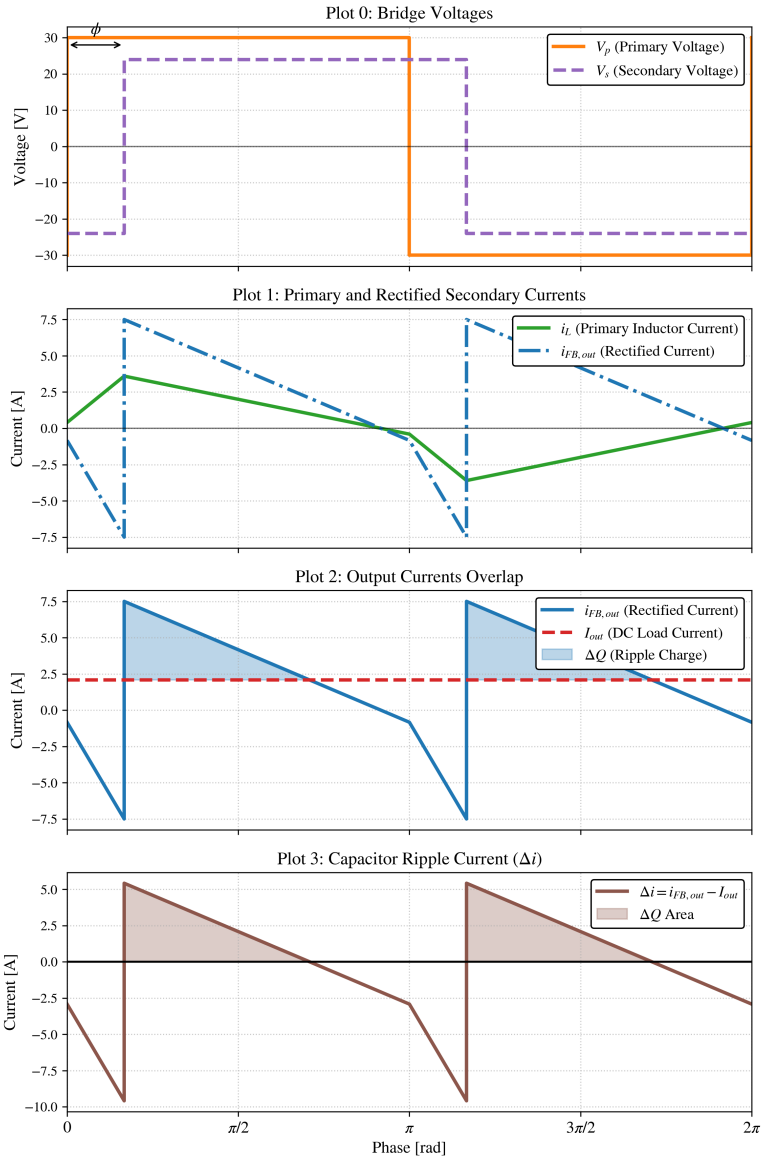


Figure 2 V_p, V_s, i_L, I_{out}, $i_{FB,out}$, Δi and ΔQ.

I_{out} = 2.08 A	I_1 = 3.6 A	I_2 = −0.4 A	$\Delta Q = 2.94 \times 10^{-6}$ C	$C_{out} = 6.12 \times 10^{-6}$ F	/ 10 pt.

Q6: PLECS VALIDATION FOR THE OUTPUT VOLTAGE RIPPLE

Using the provided PLECS model `Q6.plecs`, enter your DAB converter parameters. Verify that the output voltage ripple meets the requirements during the operation with the minimum input voltage. Please show the following waveforms:

a) Current of the inductor i_L
b) Output current of the secondary side full bridge $i_{FB,out}$
c) Output voltage v_{out}

NOTE: Please show only three switching periods after the signals reach steady state.

Also, write down your output voltage peak-to-peak ripple.

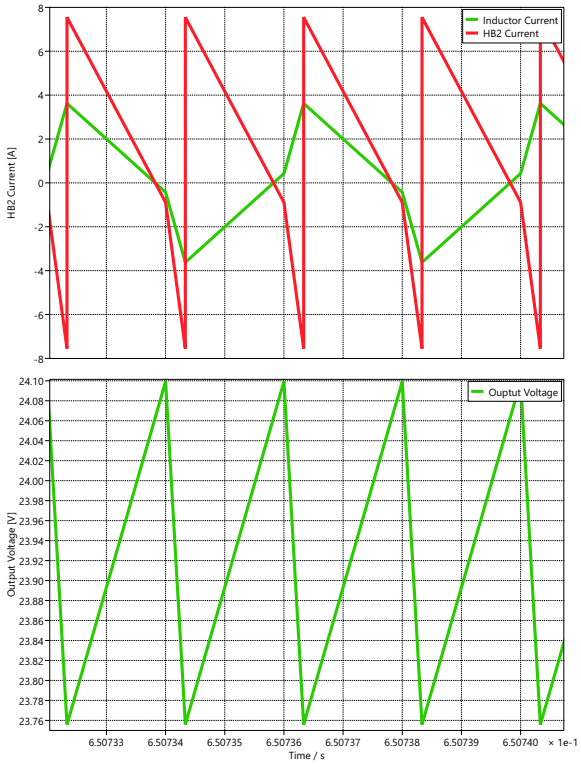


Figure 3 Voltage and current waveforms of interest.

The peak to peak voltage is $24.1 - 23.75 = 0.35V$

$V_{out,ripple}$ = 0.35 V

/ 2 pt.

Q7: CURRENT OF THE OUTPUT CAPACITOR, I_{COUT}

Using the simulation from Q6, obtain and present the waveform of the output capacitor's current i_{Cout}. Obtain the RMS value $I_{Cout,RMS}$ using PLECS built in calculation blocks.

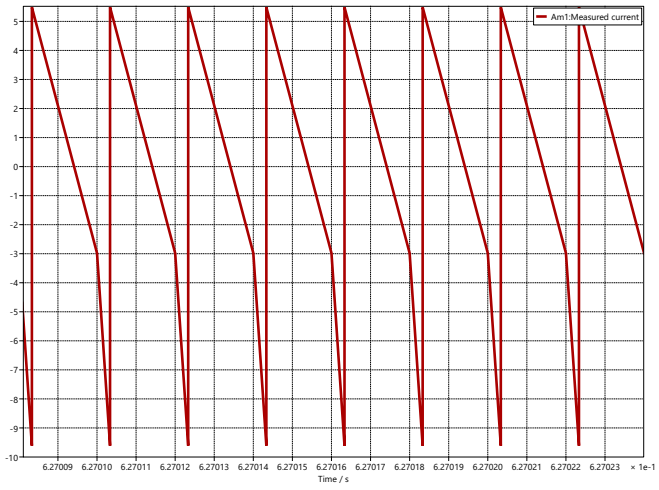


Figure 4 Current in the output capacitor in [A]

Its RMS value is $I_{Cout,RMS} = 3.682$ A

$I_{Cout,RMS} = 3.68$ A

/ 2 pt.

Q8: DC BLOCKING CAPACITOR, $C_{DCBLOCK}$

DC Blocking capacitors are introduced in the power stage to avoid saturation of the transformer due to dead-time impact or unbalanced currents, especially during start-up and load transients. The DC capacitor should not affect the switch node voltage in a significant manner. A good starting value can be determined using provided equation.

$$C_{DCblock,min} = \frac{100}{4 \times \pi^2 \times f_{sw}^2 \times L} \tag{2}$$

$$C_{DCblock,min} = \frac{100}{4 \times \pi^2 \times f_{sw}^2 \times L} = 4.8654 \times 10^{-6} F$$

$C_{DCBlock,min} = 4.86 \times 10^{-6} F$

/ 2 pt.

Q9.1: INPUT CAPACITANCE DEFINED BY VOLTAGE RIPPLE, $C_{IN,RIPPLE}$

Consider 2 % of voltage ripple tolerance, similar with the calculation in Q5. Calculate the DC input current I_{in} and the current which goes to the primary side H-bridge stage $i_{FB,pri}$. The difference of these currents causes the voltage ripple on the capacitance $C_{in,ripple}$.

The worst-case input ripple occurs when the input current is at its highest, meaning at the minimum input voltage $U_{in,min} = 30$ V and nominal power $P = 50$ W.

1. **DC Input Current**: $I_{in} = \frac{P}{U_{in,min}} = \frac{50}{30} = 1.667$ A.
2. **Primary H-Bridge Current ($i_{FB,pri}$)**: During the first half-cycle (from 0 to 2μs : When Q1 and Q4 are active), $i_{FB,pri}$ is identical to the primary inductor current i_L. It starts at $-I_2 = 0.40$ A, rises to its peak $I_1 = 3.60$ A, and drops back to $I_2 = -0.40$ A.
3. **Ripple Charge (ΔQ_{in})**: The capacitor provides charge when $i_{FB,pri} > I_{in}$. This forms a positive triangle of excess current:
   - Peak current difference (Height): $\Delta i_{peak} = I_1 - I_{in} = 3.60 - 1.667 = 1.933$ A.
   - The rising slope is $\frac{V_p + nV_s}{L} = 9.60$ A/μs. The time from crossing I_{in} (red line) to reaching the peak is $\frac{1.933}{9.60} = 0.201$ μs.
   - The falling slope is $\frac{V_p - nV_s}{L} = -2.40$ A/μs. The time to drop from the peak back down to I_{in} is $\frac{-1.933}{-2.40} = 0.805$ μs.
   - Total duration of excess current (Base): $\Delta t = 0.201 + 0.805 = 1.006$ μs.

   Integrating this triangle gives the ripple charge:
   $\Delta Q_{in} = \frac{1}{2} \times 1.933 \text{ A} \times 1.006 \times 10^{-6}$ s $= 0.972 \times 10^{-6}$ C.
4. $C_{in,ripple}$: We are allowed a 2% ripple on the 30 V input. This gives $\Delta U_{in} = 0.02 \times 30 = 0.60$ V.
   $C_{in,ripple} = \frac{\Delta Q_{in}}{\Delta U_{in}} = \frac{0.973 \times 10^{-6}}{0.60} = 1.62 \times 10^{-6}$ F.

This is a picture to illustrate what happens.

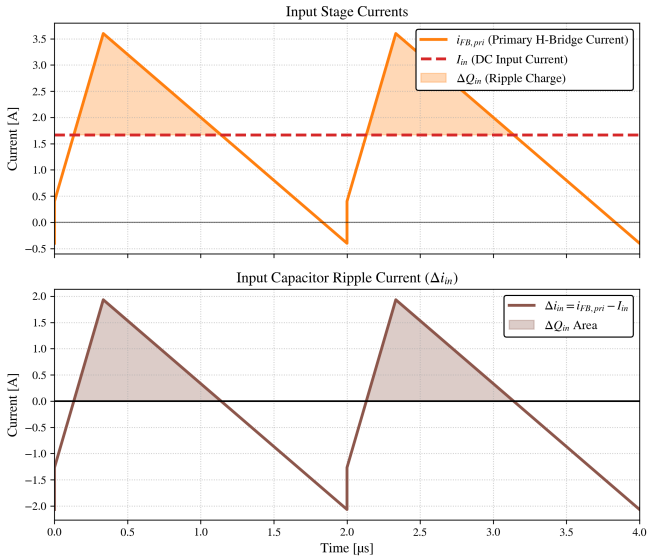


Figure 5 Input stage currents and the input capacitor ripple charge ΔQ_{in}.

$C_{in,ripple} = 1.62 \times 10^{-6}$ F

/2 pt.

Q9.2: INPUT CAPACITANCE DEFINED BY HOLD-UP TIME, $C_{IN,HOLDUP}$

In some applications, there may be an AC-DC converter that provides the input voltage to the DAB converter. In case that there is an grid outage (loss of AC supply), there needs to be sufficient installed energy in the capacitance between AC-DC and DC-DC DAB converter, allowing for uninterrupted operation and power delivery to the load at DAB output. This requirement is usually referred to as hold-up time. While in your project, we do not have AC-DC stage before DAB, we can still consider this scenario and calculate required energy or capacitance.

Calculate the minimum required capacitance so that, in case of a half-cycle grid's interruption (10 ms), the DAB output voltage remains within the limits, while the converter outputs its rated power. Consider the scenario where the input voltage is allowed to drop from the rated value to the minimum value during 10 ms, while the converter delivers rated power to the load.

During a grid outage, the input capacitor must supply the total energy required by the load for the hold-up duration $t_{holdup} = 10$ ms.

- The energy consumed by the converter delivering nominal power is:

$$E_{req} = P_{out,nom} \times t_{holdup} = 50\ \text{W} \times 10 \times 10^{-3}\ \text{s} = 0.5\ \text{J}$$

- The input capacitor discharges from its nominal voltage ($U_{in,nom} = 50$ V) down to the minimum allowed operational voltage ($U_{in,min} = 30$ V). The usable energy it releases is:

$$\Delta E_{cap} = \frac{1}{2} C_{in,holdup} \left(U_{in,nom}^2 - U_{in,min}^2 \right)$$

- The released energy should be equal to the energy consumed by the converter :

$$0.5\ \text{J} = \frac{1}{2} C_{in,holdup} \left(50^2 - 30^2 \right) = \frac{1}{2} C_{in,holdup} (2500 - 900)$$

$$0.5 = C_{in,holdup} \times 800$$

$$C_{in,holdup} = \frac{0.5}{800} = 625 \times 10^{-6}\ \text{F}$$

$C_{in,holdup} = 625 \times 10^{-6}$ F

/2 pt.

Q10: DISCHARGE RESISTANCE

A discharge resistance is connected in parallel to the input capacitor to completely discharge the input capacitance when the converter is turned off. This is a safety feature, which prevents the risk of electrical shock to the body of curios humans, interested to hold your DAB converter in their hands.

Determine the required resistance $R_{discharge}$ to completely discharge the input capacitance from 100% to 5% of the rated voltage in less than 1 minute.

Presence of this resistor will cause a constant power loss in operation and impact your DAB efficiency. Calculate the power loss $P_{loss,Rdischarge}$ of this resistor when working with maximum input voltage.

For ease of notation, lwt's denote $C_{in,ripple}$ as C and $t_{discharge}$ as t_1 with $t_1 = 60$ s and $C = 1.62 \times 10^{-6}$ F
The discharge of the capacitor is characterized by the equation: : $V(t) = V_0\, e^{-t/(RC)}$
We require the voltage to drop to 5% of its initial value in $t_1 = 60$ s: $V(t_1) = 0.05\, V_0 = V_0\, e^{-t_1/(RC)}$
$\Rightarrow 0.05 = e^{-t_1/(RC)} \Rightarrow t_1/(RC) = -\ln(0.05)$

$$R_{discharge} = -\frac{t_1}{C\ln(0.05)} = \frac{-60}{1.62\times10^{-6}\,.\,\ln(0.05)} = 1.236 \times 10^7\ \Omega = 12.36 \times 10^6\ \Omega$$

$$P_{loss,Rdischarge} = \frac{V_{in,max}^2}{R_{discharge}} = \frac{60^2}{12.36\times10^6} = 2.91 \times 10^{-4}\ \text{W}$$

$R_{discharge} = 12.36\ \text{M}\Omega$ | $P_{loss,Rdischarge} = 2.91 \times 10^{-4}$ W | /4 pt.

Q11: PLECS VALIDATION FOR MAXIMUM AND MINIMUM INPUT VOLTAGE

Now that you have determined the values of all relevant components, enter your parameters into the provided PLECS model `Q11.plecs` of the DAB converter. Verify the results for the maximum input voltage. For this purpose, include the following waveforms:

a) Transformer primary and secondary side voltage
b) Voltage and current across the inductor L
c) Voltage across the DC blocking capacitor $C_{DCblock}$
d) Current of the output capacitor C_{out}
e) Output voltage and output current

The values used for the simulations are : $L = 8.33 \times 10^{-6}$ H, $N = 2.083$, $f_{sw} = 250 \times 10^3$ Hz, $C_{out} = 6.12 \times 10^{-6}$ F, $C_{DCblock} = 4.86 \times 10^{-6}$ F.
Figure 6 shows all of the waveforms for the minimum input voltage $V_{min} = 30$ V and corresponding phase $\varphi_{min} = 0.52$ rad.
Figure 7 shows all of the waveforms for the maximum input voltage $V_{min} = 60$ V and corresponding phase $\varphi_{max} = 0.24$ rad.

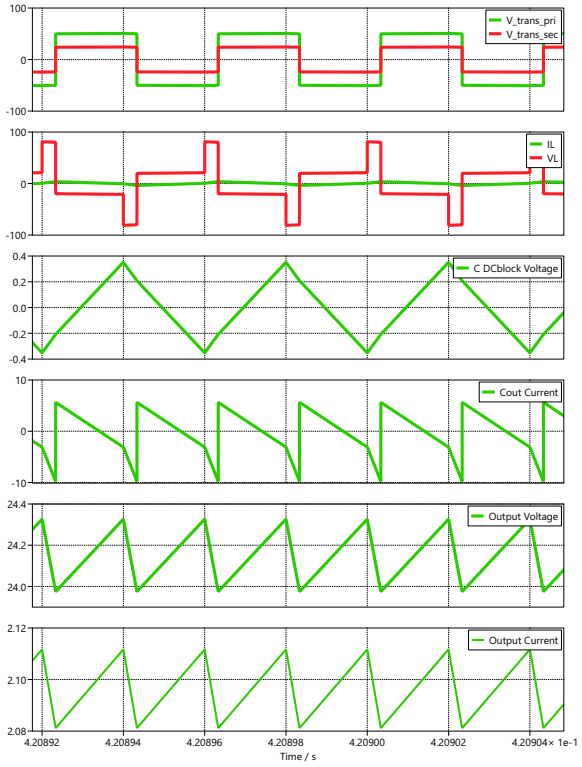


Figure 6 Voltage and current waveforms of interest with minimum input voltage.

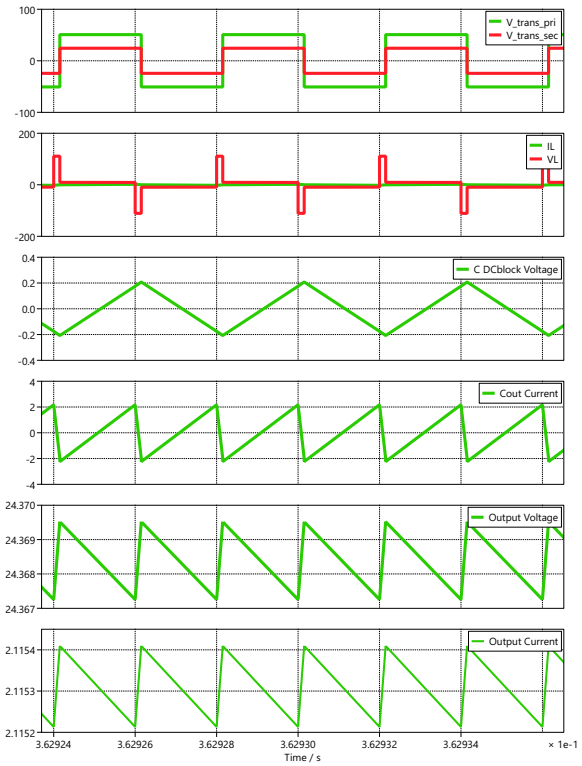


Figure 7 Voltage and current waveforms of interest with maximum input voltage.

/ 5 pt.

Q12: PLECS VALIDATION FOR $\frac{1}{4}$ OF THE NOMINAL POWER

In Q11, you validated your converter design when the input voltage is at its maximum and minimum. In addition to these operating points, your DAB converter must be able to regulate the output voltage within the specific voltage and power ranges. To validate that, analyze the simulation results for the minimum input voltage at 1/4 of the nominal power. You have to re-calculate the phase shift $\varphi_{\frac{1}{4}}$ by Equation1. Please update these values in the PLECS simulation files.
Then show the following waveforms:

a) Transformer primary and secondary side voltage
b) Voltage and current across the inductor L
c) Voltage across the DC blocking capacitor $C_{DCblock}$
d) Current of the output capacitor C_{out}
e) Output voltage and output current
f) Voltage and gate signal of one MOSFET

Comment briefly on your observations on the graphs: What is the voltage across the selected MOSFET? Is ZVS still achieved?

Let's use the equation : $P_{\frac{1}{4}} = \frac{nU_{min}V_{sec}\varphi_{\frac{1}{4}}(\pi - |\varphi|_{\frac{1}{4}})}{2\pi^2 f_{sw}L}$

We get that : $\varphi_{\frac{1}{4}}(\pi - \varphi_{\frac{1}{4}}) = \frac{2.P_{\frac{1}{4}}.\pi^2 f_{sw}.L}{n.U_{min}.V_{sec}} = \frac{2\times12.5\times\pi^2\times250\times10^3\times8.33\times10^{-6}}{2.08\times30\times24} = 0.343$ with $\varphi_{\frac{1}{4}} > 0$.
We finally get that $\varphi_{\frac{1}{4}} = 0.1132$ rad or $\varphi_{\frac{1}{4}} = 3.028$ rad. We use $\varphi_{\frac{1}{4}} = 0.1132$.

Figure 8 and figure 9 show the interest waveforms for the case of minimal input voltage $V_{min} = 30$ V and 1/4 of the nominal power $P_{\frac{1}{4}} = 12.5$ W. They represent simulations of the circuit with zero and $20ns$ switching dead time, respectively.
(V_{DS1}, V_{GS1}), V_{GS2}, V_{GS5} and V_{GS6} and are measured for P1, P3, S1 and S3 (Q1, Q2, Q5 and Q6 in the slides) respectively.
Observations :

- The voltage across the MOSFET P1 (V_DS1) oscillates between 0 and 30V.
- In the ideal simulation with zero dead time, V_{DS1} drops instantly at the exact moment the gate signal turns on. This represents ideal hard-switching, not Zero Voltage Switching (ZVS). For ZVS to be achieved, the voltage must naturally discharge to 0 V during a dead-time period prior to the gate turning on. Because the PLECS model uses ideal switches without any parasitic capacitances, the passive discharge required for ZVS cannot be observed here. In a physical circuit at 1/4 power, the inductor current is generally too low to fully discharge the parasitic capacitances, meaning ZVS would be lost.
- We can see that in figure 9, the output voltage no longer oscillates around 24V, but varies around 17.6V instead. This is explained by the dead-time added, that would require a modification of φ by the controller. Because, φ, was kept the same as before, the output voltage decreases.

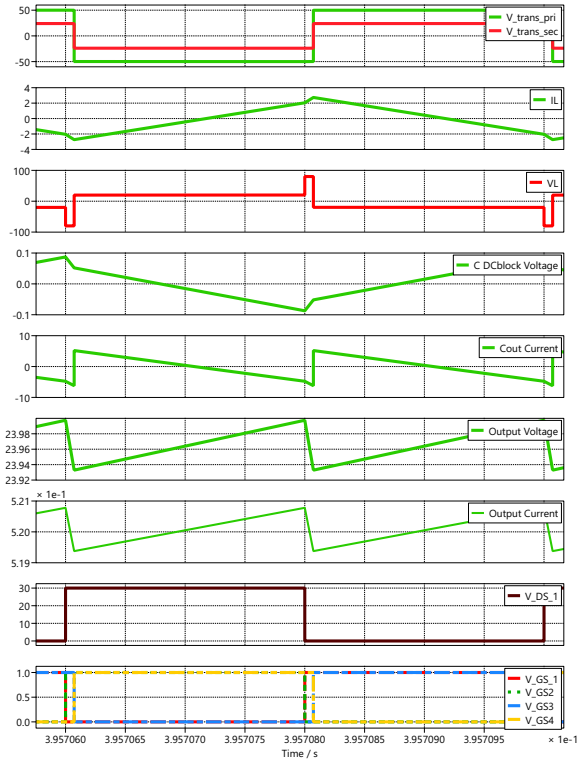


Figure 8 Voltage and current waveforms of interest with $t_{dead} = 0$ s.

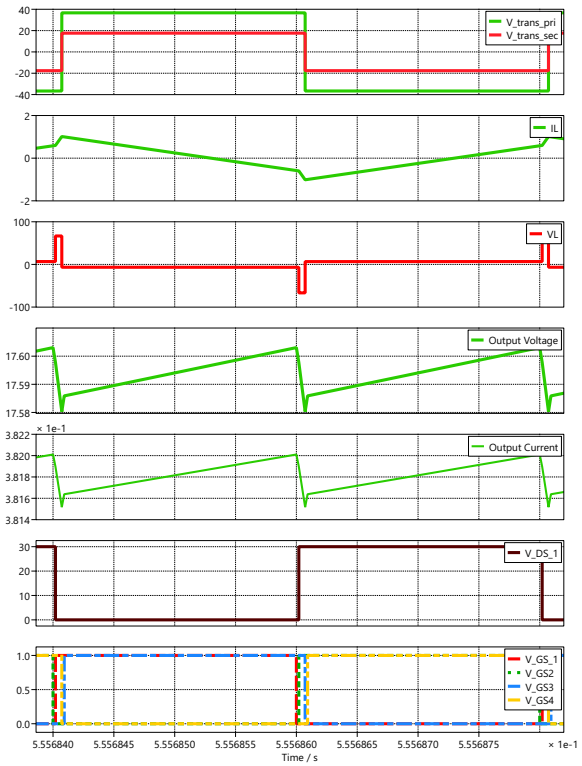


Figure 9 Voltage and current waveforms of interest with $t_{dead} = 20$ ns.

$\varphi_{\frac{1}{4}} = 0.1132$ rad

/ 5 pt.

SELECTION OF SEMICONDUCTORS

The second part of this report focuses on the selection of semiconductor devices for your design. You will have to derive equations for your design, eventually leading to the selection of proper semiconductors that you will use in your design. As in the first set of questions, provide numeric answers with a precision of two digits after the decimal point in the provided unit.

Q13: PRIMARY SIDE SEMICONDUCTOR STRESSES

To select an appropriate MOSFET for your design, you need to determine the maximum voltage and current stress that it has to handle in your circuit under the worst-case operating conditions. For this purpose, provide:

a) The maximum voltage across the primary-side MOSFET $U_{Q,pri,max}$;
b) The maximum current flowing through the primary side MOSFET $I_{Q,pri,max}$.

Parasitic effects cause voltage overshoots that can damage the device. To estimate these effects, a good practice is to scale up the maximal voltage stress by a factor of 1.5.

Obtain the maximum voltage stress and maximum current by theoretical calculation first, then verify them by the simulation in the previous section. In your answer, indicate the working scenario from which you obtained $U_{Q,pri,max}$ and $I_{Q,pri,max}$. Then, considering the voltage safety factor of 1.5, give the final answer for the maximum voltage stress.

The maximum voltage accros the primary side transistor is simply the maximum input voltage $U_{in,max} = 60$V. With the safety factor, we get $U_{Q,pri,max} = 90$ V.

The maximum current was already found in Q5.2 and is the current $I_1 = 3.6$ A, with the safty factor : $I_{Q,pri,max} = 5.4$A.

We observe similar results in the simulation

$U_{Q,pri,max} = 90$ V | $I_{Q,pri,max} = 5.4$ A | / 4 pt.

Q14: PRIMARY SIDE SEMICONDUCTOR SELECTION

Based on the obtained values from Q13, select one specific MOSFET device for your design from the offered lists in Table 2. Elaborate briefly on why you chose exactly this models and highlight it in the Table, as exemplified for the first device.
NOTE: Please do NOT choose device 9 as the maximum gate voltage is 5 V, and the gate drive voltage is designed to be 12 V this year.

Using the conditions obtained from the previous question and analyzing Table 2, we conclude that transistors 1, 2, and 6 are the best choices. They comfortably satisfy the voltage and current requirements while offering the lowest $R_{ds,on}$ to minimize conduction losses. Since all three devices share the same TO-220 package footprint and have similar pricing, physical size and cost are not the deciding factors here. However, while devices 1 and 2 offer a slightly lower $R_{ds,on}$, they are rated for 200 V. Using devices with a voltage rating this much higher than our 90 V maximum stress usually implies larger silicon die areas and higher parasitic capacitances. This increases dynamic switching losses and makes Zero Voltage Switching (ZVS) harder to achieve.

Conclusion: We choose the Nexperia PHP18NQ11T (No. 6). Its 110 V and 13 A ratings safely exceed our limits with a suitably low on-resistance.

MOSFET model No. : 6 | / 4 pt.

Table 2 The list of offered MOSFET devices. The parameter U_{ds} is the rated drain-source voltage, whereas the I_{cont} stands for continuous drain-source current. All devices are in the TO-220 package (see Fig. 10).

No.	Manufacturer	Product	$U_{ds,max}$ (V)	I_{cont} (A)	$R_{ds,on}$ @ 25 °C (mΩ)
1	Infineon	IRFB5620PbF	200	18	60
2	Rohm	RCX300N20	200	16.3	60
3	Onsemi	FDPF18N20FT-G	200	10.8	120
4	Rohm	RCX200N20	200	10.8	100
5	Onsemi	FQPF630	200	6.3	340
6	Nexperia	PHP18NQ11T	110	13	80
7	Vishay	SiHF530	100	10	160
8	ST	STP16NF06	60	11	80
9	Infineon	IRLZ44NPBF	55	47	22
10	Infineon	IRLB8743PbF	30	110	3.2

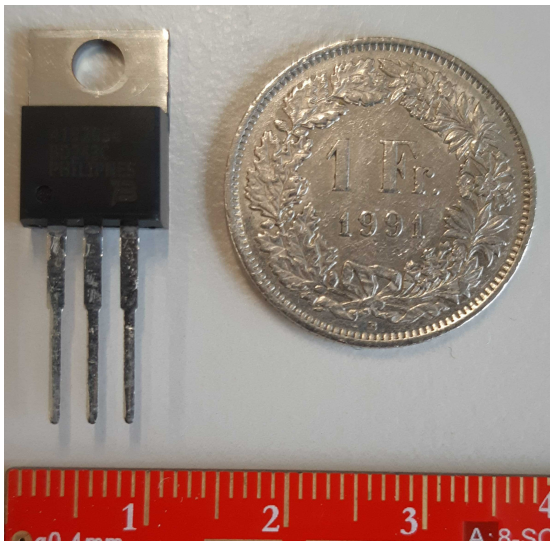


Figure 10 A semiconductor in a TO-220 case.

Q15: SECONDARY SIDE SEMICONDUCTOR STRESSES

Similarly as for the primary side, provide:

a) The maximum voltage across the secondary-side MOSFET $U_{Q,sec,max}$;
b) The maximum current flowing through the secondary-side MOSFET $I_{Q,sec,max}$.

Similarly to the primary-side devices, consider a scaling of 1.5 for the maximum voltage stress.
Obtain the maximum voltage stress and maximum current by theoretical calculation first, then verify them by the simulation in the previous section. In your answer, indicate the working scenario from which you obtained $U_{Q,sec,max}$ and $I_{Q,sec,max}$. Then, considering the voltage safety of 1.5, give the final answer for the maximum voltage stress for both the primary and secondary sides.

The maximum voltage accros the secondary side transistor is simply the maximum input voltage $U_{ou,nom} = 24$V. With the safety factor, we get $U_{secMOS,max} = 36$ V.
As for the maximum current in the secondary transistors we have : $I_1 * n = 7.48$ A, with the safty factor : $I_{Q,pri,max} = 11.25$A. We observe similar results in the simulation

$U_{secMOS,max} = 36$V | $I_{secMOS,max} = 11.25$ A | / 4 pt.

Q16: SECONDARY SIDE SEMICONDUCTOR SELECTION

Based on the obtained values from Q15, select one specific MOSFET device for your design from the offered lists in Table 2. Briefly elaborate on why you chose exactly this model and highlight it in the Table, as it is exemplified for the first device.

Following the same reasoning as in Question 14, the Nexperia PHP18NQ11T (No. 6) remains the optimal choice for the secondary side. It safely satisfies the secondary voltage and current constraints ($U_{Q,sec,max} = 36$ V, $I_{Q,sec,max} = 11.25$ A) with its 110 V and 13 A ratings, while maintaining a low $R_{ds,on}$ to minimize conduction losses. Additionally, using the exact same MOSFET model for both the primary and secondary H-bridges simplifies the Bill of Materials (BoM), making the future PCB assembly process easier.

MOSFET model No. : 6 | / 4 pt.

CALCULATION OF CURRENTS' AVERAGE AND RMS VALUES

In this section, you will obtain the Average and the RMS current values for the semiconductors of the DAB converter through calculation and simulation. The results have to be given with two digits after the decimal point using the given unit.
NOTE: Ignore the DC blocking capacitor during the calculation.

Q17: CALCULATION OF THE PRIMARY SIDE MOSFET CURRENT

Consider the worst-case operating conditions and provide:

a) The plot of the current waveform of one primary side MOSFET. Select one from 4 MOSFETs, and **do NOT obtain this current waveform by simulation**.
b) The primary side MOSFET's RMS current $I_{Q,pri,rms}$;
c) The primary side MOSFET's average current $I_{Q,pri,avg}$;

In your answer, indicate the results of your $I_{Q,pri,rms}$, $I_{Q,pri,avg}$.

The current in the transistor of the primary side is simply a cut down (by the primary transistor switching) version of the current in the inductor. Thus, the waveforme are the following :

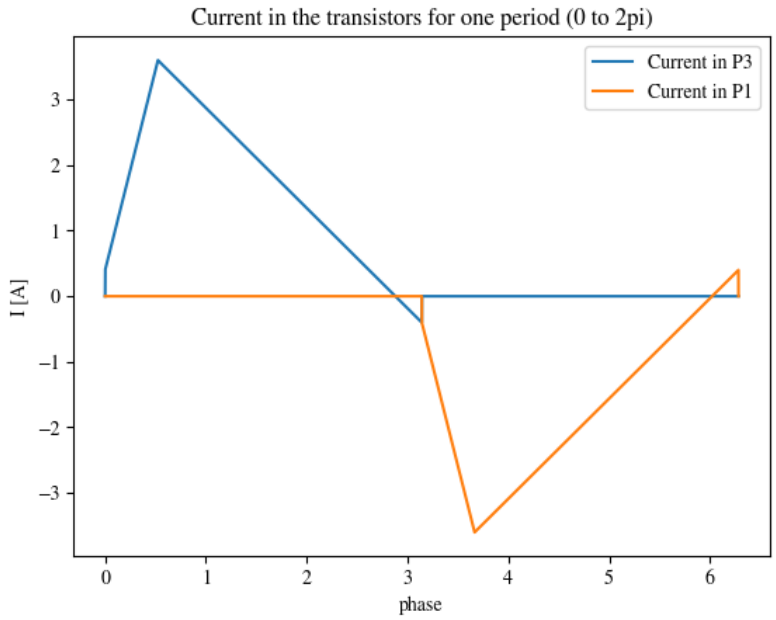


Figure 11 Current in transistor P3 (and the opposed transistor P1)

We can calculate the average and RMS values of the blue curve with our python code.

Calculation: $I_{Q,pri,rms}$ = 1.42 A $I_{Q,pri,avg}$ = 0.83 A	/ 4 pt.

Q18: PLECS SIMULATION OF THE PRIMARY SIDE MOSFET CURRENT

Using the provided PLECS model given in Q11 and considering worst-case operating conditions, show the simulation waveforms in the following box and obtain the values for:

a) The primary side MOSFET's RMS current $I_{Q,pri,rms}$;
b) The primary side MOSFET's average current $I_{Q,pri,avg}$;

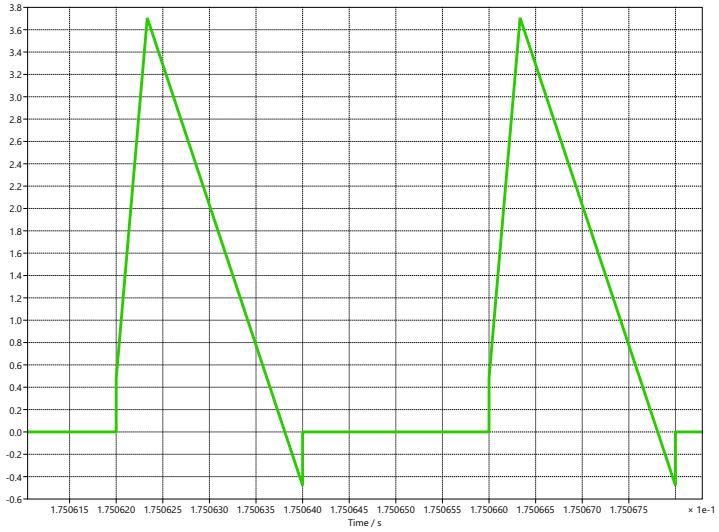


Figure 12 Current in transistor P3

The values for $I_{Q,pri,rms}$ and $I_{Q,pri,avg}$ were found using the built in RMS and average module.

Simulation: $I_{Q,pri,rms}$ = 1.47 A $I_{Q,pri,avg}$ = 0.86 A	/ 4 pt.

Q19: CALCULATION OF THE SECONDARY SIDE MOSFET CURRENT

Consider the worst-case operating conditions and provide:

a) Plot the current waveform of the secondary side MOSFET. Select one from 4 devices, and do NOT obtain this current waveform by simulation.
b) The secondary side MOSFET's RMS current $I_{Q,sec,rms}$;
c) The secondary side MOSFET's average current $I_{Q,sec,avg}$;

In your answer, indicate the results of your $I_{Q,sec,rms}$, $I_{Q,sec,avg}$.

The current in the transistor of the secondary side is simply a cut down (by the secondary transistor switching) version of the current in the inductor, scaled by a factor n. Thus, the waveform are the following :

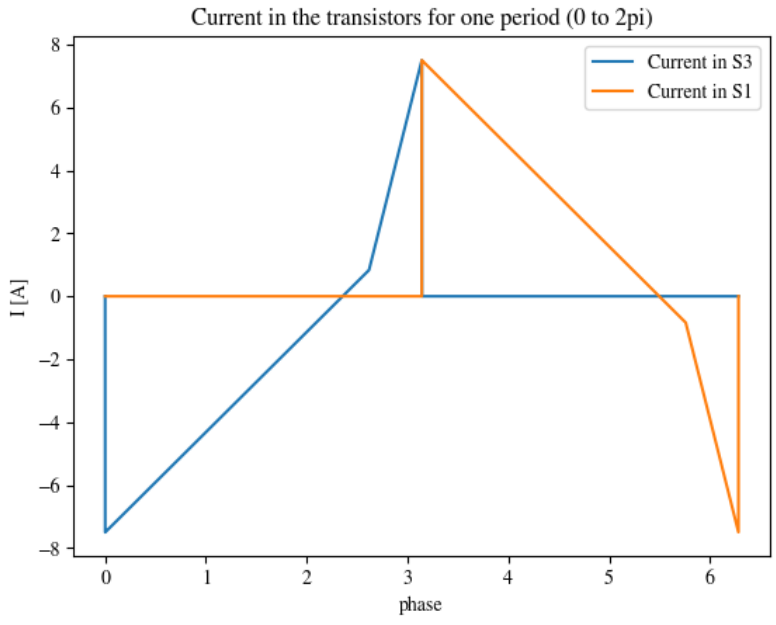


Figure 13 Current in transistor S3 (and opposed transistor S1)

We can calculate the average and RMS values of the blue curve with our python code.

Calculation: $I_{Q,sec,rms}$ = 2.97 A $I_{Q,sec,avg}$ = -1.04 A

/ 4 pt.

Q20: PLECS SIMULATION OF THE SECONDARY SIDE MOSFET CURRENT

Using the provided PLECS model given in Q11, consider worst-case operating conditions, show the simulation waveforms, and obtain the values for:

a) The secondary side MOSFET's RMS current $I_{Q,sec,rms}$;
b) The secondary side MOSFET's average current $I_{Q,sec,avg}$;

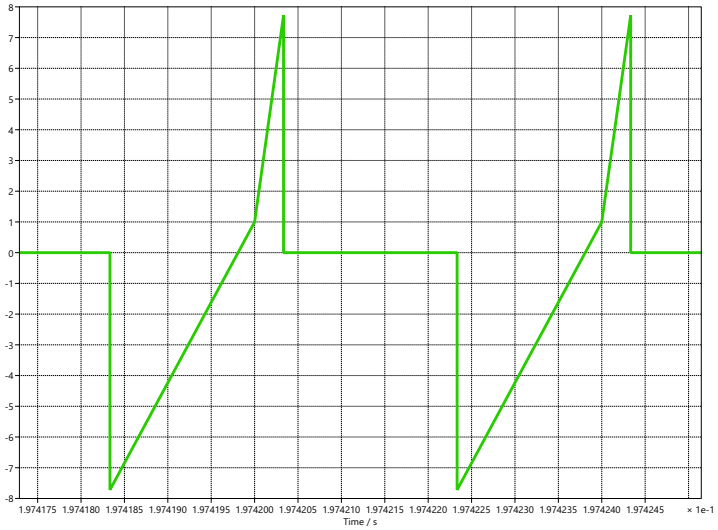


Figure 14 transistor S3 Current

The values for $I_{Q,sec,rms}$ and $I_{Q,sec,avg}$ were found using the built in RMS and average module.

Simulation: $I_{Q,sec,rms}$ = 3.06 A $I_{Q,sec,avg}$ = -1.06 A

/ 4 pt.

SEMICONDUCTOR LOSSES AND THERMAL DESIGN

Using your previous results, semiconductor losses can be calculated and compared with the provided MATLAB Loss Tool. The results using the worst case (provided by the Loss Tool) will be used to help you select appropriate heatsinks for your design. As in the other questions, results should be given with two digits after the decimal point in the unit indicated. The Infineon Application Notes should be used as a guideline for questions Q21 to Q24.

Q21: PRIMARY SIDE MOSFET CONDUCTION LOSSES

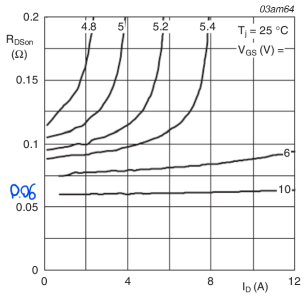
Using the datasheet of your selected MOSFET as well as the results from your simulations from Q19, calculate the MOSFET conduction losses at steady state under worst-operating conditions (I_{max} and $U_{in,min}$). The MOSFETs are assumed to operate with a junction temperature of 125 °C.

Using the datasheet of our transistors (assuming a V_{GS} of 10 V and a temperature of 125°C), we get a R_{on} of 0.12 Ω (see left plot of figure 15).
The rms current in the primary transistor was $I_{Q,pri,rms}$ = 1.47 A.
The steady state losses are thus

$$P_{Q,pri,cond} = I^2_{Q,pri,rms} \times R_{on} = 1.47^2 \times 0.12 = 0.26\ \text{W}$$

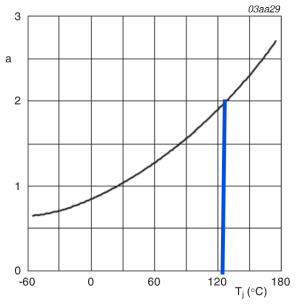
Nexperia **PHP18NQ11T**

N-channel TrenchMOS standard level FET



$T_j = 25°C$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature

Figure 15 figures from our transistor datasheet

$P_{Q,pri,cond}$ = 0.26 W

/ 4 pt.

Q22: SECONDARY SIDE MOSFET CONDUCTION LOSSES

Using the datasheet of your selected MOSFET as well as the results from your simulations from Q21, calculate the MOSFET conduction losses at steady state under worst-operating conditions (I_{max} and $U_{in,min}$). The MOSFETs are assumed to operate at a junction temperature of 125 °C.

Similarly to last question, we get a R_{on} of 0.12 Ω.
The rms current in the secondary transistor was $I_{Q,sec,rms}$ = 3.06 A.
The steady state losses are thus $P_{Q,sec,cond} = I^2_{Q,sec,rms} \times R_{on} = 3.06^2 \times 0.12 = 1.12\text{W}$

$P_{Q,sec,cond}$ = 1.12 W

/ 4 pt.

Q23: PRIMARY SIDE MOSFET SWITCHING LOSSES

Using again the datasheet and your previous simulation results, calculate the primary side MOSFET turn-on and turn-off losses $P_{T,on}$, $P_{T,off}$, at steady state under worst-case operating conditions, that is, the conditions resulting in higher switching losses. For that, iterate in your calculations and find the conditions that yield higher switching losses and comment them in your solution.

NOTE 1: Remember that the converter is expected to always operate in ZVS, which will simplify your transistor switching losses calculations. In practice, if ZVS is lost in the operation, switching losses will increase.
NOTE 2: You will need to obtain from simulation the **turn-off** current of the MOSFET.
NOTE 3: Please consider the gate drive voltage as 12 V and gate resistance as 5 Ω

In your answer, explain how did you find the worst-case operating conditions and indicate which operating condition you got the results from.

Turn-on losses :
As the converter is designed to operate under Zero Voltage Switching (ZVS), the dead time is such that the parasitic capacitances are discharged passively. This forces V_{DS} to 0 V before switching on the transistor, thus leading to turn-on losses of 0 W

Turn-off losses :
We will compute the turn-off losses for both cases of $U_{in} = 30$ V and $U_{in} = 60$ V.

- We have from the previous questions that $R_{DSon} = 0.12\,\Omega$
- From **NOTE 3**, we get : $U_{Dr} = 12$ V and $R_G = 5\,\Omega$.

From the data sheet we get the following parameter values :

- **Fall time :** $t_f = 12$ **ns**
- **Gate Plateau Voltage** $U_{plateau} = 5$ **V**

1. **For** $U_{in} = 60$ **V :**
   - We get from the PLECS simulation $I_{on} = 2.058$ A.
   - **Gate-Drain Capacitance :**
     - At $V_{DS} = 60V$: $C_{GD1} = 40$ pF.
     - at $V_{DS} = R_{DSon} \times I_{on} = 0.12 \times 2.058 = 0.247$ V $\Rightarrow C_{GD2} = 400$ pF

   $t_{ru_1} = (U_{in} - R_{DSon} \times I_{on}) \cdot R_G \cdot \frac{C_{GD1}}{U_{plateau}} = (60 - 0.247) \times 5 \times \frac{40 \times 10^{-12}}{5} = 2.3901 \times 10^{-9}$ s ≈ 2.39 ns

   $t_{ru_2} = (U_{in} - R_{DSon} \times I_{on}) \cdot R_G \cdot \frac{C_{GD2}}{U_{plateau}} = (60 - 0.247) \times 5 \times \frac{400 \times 10^{-12}}{5} = 2.3901 \times 10^{-8}$ s ≈ 23.9 ns

   $t_{ru} = \frac{t_{ru_1} + t_{ru_2}}{2} = \frac{2.39 + 23.9}{2} \times 10^{-9} = 13.15$ ns

   The turn-off energy is:

$$E_{offM} = U_{in} \cdot I_{on} \cdot \frac{t_{ru} + t_f}{2} = 60 \times 2.058 \times \frac{13.15 + 12}{2} \times 10^{-9} \approx 1.55 \times 10^{-6} \text{J}$$

   The total turn-off power loss is:

$$P_{Q,pri,off} = E_{offM} \cdot f_{sw} = 1.55 \times 10^{-6} \times 250,000 \text{ Hz} = 0.39 \text{ W}$$

2. **For** $U_{in} = 30$ **V :**
   - We get from the PLECS simulation $I_{on} = 0.48$ A.
   - **Gate-Drain Capacitance :**
     - At $V_{DS} = 30V$: $C_{GD1} \approx 54$ pF.
     - at $V_{DS} = R_{DSon} \times I_{on} = 0.12 \times 0.48 = 0.058$ V $\Rightarrow$ we take the lowest value of the datasheet plot (for $V_{DS} = 10^{-1}$ V). We get : $C_{GD2} = 500$ pF

   $t_{ru_1} = (U_{in} - R_{DSon} \times I_{on}) \cdot R_G \cdot \frac{C_{GD1}}{U_{plateau}} = (30 - 0.058) \times 5 \times \frac{54 \times 10^{-12}}{5} = 1.62 \times 10^{-9}$ s $= 1.62$ ns

   $t_{ru_2} = (U_{in} - R_{DSon} \times I_{on}) \cdot R_G \cdot \frac{C_{GD2}}{U_{plateau}} = (30 - 0.058) \times 5 \times \frac{500 \times 10^{-12}}{5} = 14.97 \times 10^{-9}$ s $= 14.97$ ns

   $t_{ru} = \frac{t_{ru_1} + t_{ru_2}}{2} = \frac{1.62 + 14.97}{2} \times 10^{-9} = 8.29$ ns

   The turn-off energy is:

$$E_{offM} = U_{in} \cdot I_{on} \cdot \frac{t_{ru} + t_f}{2} = 30 \times 0.48 \times \frac{8.29 + 12}{2} \times 10^{-9} \approx 1.46 \times 10^{-7} \text{J}$$

   The total turn-off power loss is:

$$P_{Q,pri,off} = E_{offM} \cdot f_{sw} = 1.46 \times 10^{-7} \times 250,000 \text{ Hz} = 0.037 \text{ W}$$

   The worse case scenario is the case of $U_{in} = 60$ V.

$P_{Q,pri,on}$ = 0 W	$P_{Q,pri,off}$ = 0.39 W	/ 8 pt.

Q24: SECONDARY SIDE MOSFET SWITCHING LOSSES

Using again the datasheet and your previous simulation results, calculate the secondary side MOSFET turn-on and turn-off losses $P_{T,on}$, $P_{T,off}$, at steady state under worst-case operating conditions, that is, the conditions resulting in higher switching losses. For that, iterate in your calculations and find the conditions that yield higher switching losses and comment them in your solution.

NOTE 1: Remember that the converter is expected to always operate in ZVS, which will simplify your transistor switching losses calculations. In practice, if ZVS is lost in the operation, switching losses will increase.
NOTE 2: You will need to obtain from simulation the **turn-off** current of the MOSFET.
NOTE 3: Please consider the gate drive voltage as 12 V and gate resistance as 5 Ω

In your answer, explain how did you find the worst-case operating conditions and indicate which operating condition you got the results from.

Turn-on losses :
Same explanation as in the last question : As the converter is designed to operate under Zero Voltage Switching (ZVS), the dead time is such that the parasitic capacitance is discharged passively. This forces V_{DS} to 0 V before switching on the transistor, thus leading to turn-on losses of 0 W

Turn-off losses :
We will compute the turn-off losses for both cases of U_{in} = 30 V and U_{in} = 60 V. This is because the input voltage leads to a different switching current in the transistors of the secondary side.

- We have from the previous questions that $R_{DSon} = 0.12\,\Omega$
- From **NOTE 3**, we get : $U_{Dr} = 12$ V and $R_G = 5\,\Omega$.

From the data sheet we get the following parameter values :

- **Fall time :** $t_f = 12$ **ns**
- **Gate Plateau Voltage** $U_{plateau} = 5$ **V**

1. **For** $U_{in} = 60$ **V :**
   - We get from the PLECS simulation $I_{on} = 0.118$ A.
   - **Gate-Drain Capacitance :**
     - At $V_{DS} = 24V$: $C_{GD1} = 60$ pF.
     - At $V_{DS} = R_{DSon} \times I_{on} = 0.12 \times 0.118 = 0.014$ V $\Rightarrow C_{GD2} = 500$ pF

   $t_{ru_1} = (U_{sec} - R_{DSon} \times I_{on}) \cdot R_G \cdot \frac{C_{GD1}}{U_{plateau}} = (24 - 0.014) \times 5 \times \frac{60 \times 10^{-12}}{5} = 1.439 \times 10^{-9}$ s ≈ 1.44 ns

   $t_{ru_2} = (U_{sec} - R_{DSon} \times I_{on}) \cdot R_G \cdot \frac{C_{GD2}}{U_{plateau}} = (24 - 0.014) \times 5 \times \frac{500 \times 10^{-12}}{5} = 1.1992 \times 10^{-8}$ s ≈ 12 ns

   $t_{ru} = \frac{t_{ru_1} + t_{ru_2}}{2} = \frac{1.44+12}{2} \times 10^{-9} = 6.72$ ns

   The turn-off energy is:

$$E_{offM} = U_{sec} \cdot I_{on} \cdot \frac{t_{ru} + t_f}{2} = 24 \times 0.118 \times \frac{6.72 + 12}{2} \times 10^{-9} \approx 2.65 \times 10^{-8} \text{J}$$

   The total turn-off power loss is:

$$P_{Q,pri,off} = E_{offM} \cdot f_{sw} = 2.65 \times 10^{-8} \times 250,000 \text{ Hz} = 0.0066 \text{ W}$$

2. **For** $U_{in} = 30$ **V :**
   - We get from the PLECS simulation $I_{on} = 7.72$ A.
   - **Gate-Drain Capacitance :**
     - At $V_{DS} = 24V$: $C_{GD1} \approx 60$ pF.
     - at $V_{DS} = R_{DSon} \times I_{on} = 0.12 \times 7.72 = 0.93$ V $\Rightarrow C_{GD2} \approx 230$ pF

   $t_{ru_1} = (U_{sec} - R_{DSon} \times I_{on}) \cdot R_G \cdot \frac{C_{GD1}}{U_{plateau}} = (24 - 0.93) \times 5 \times \frac{60 \times 10^{-12}}{5} = 1.3844 \times 10^{-9}$ s ≈ 1.38 ns

   $t_{ru_2} = (U_{sec} - R_{DSon} \times I_{on}) \cdot R_G \cdot \frac{C_{GD2}}{U_{plateau}} = (24 - 0.93) \times 5 \times \frac{230 \times 10^{-12}}{5} = 5.307 \times 10^{-9}$ s ≈ 5.31 ns

   $t_{ru} = \frac{t_{ru_1} + t_{ru_2}}{2} = \frac{1.38+5.31}{2} \times 10^{-9} = 3.35$ ns

   The turn-off energy is:

$$E_{offM} = U_{sec} \cdot I_{on} \cdot \frac{t_{ru} + t_f}{2} = 24 \times 7.72 \times \frac{3.35 + 12}{2} \times 10^{-9} \approx 1.42 \times 10^{-6} \text{J}$$

The total turn-off power loss is:

$$P_{Q,pri,off} = E_{offM} \cdot f_{sw} = 1.42 \times 10^{-6} \times 250,000 \text{ Hz} = 0.36 \text{ W}$$

The worse case scenario is the case of $U_{in} = 30$ V.

$P_{Q,sec,on} = 0$ W	$P_{Q,sec,off} = 0.36$ W	/ 8 pt.

Q25: SEMICONDUCTOR EFFICIENCY

At this time, the losses of the semiconductors are known, calculate the efficiency η of your converter with the nominal power, when only semiconductor losses are considered. Please note that there will be other losses in your converter that will appear during the following stages of the design. You already have losses due to discharge resistor calculated in Q10. Nevertheless, semiconductor losses are dominant factor and are a good indication of the overall converter performance.

In order to compute the worse case scenario for the efficiency, we consider the highest conduction losses (at $U_{in} = 30$ V) and switching losses for both primary and secondary transistor. This means that we considered $P_{Q,pri,off} = 0.39$ which is achieved for $U_{in} = 60$ V. and $P_{Q,sec,off} = 0.36$ which is achieved for $U_{in} = 30$ V (Even though technically, both are not possible at the same time).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_{out} + P_{switch} + P_{cond}} = \frac{50}{50 + (4 \times 0.39 + 4 \times 0.36) + (4 \times 0.26 + 4 \times 1.12)} = \frac{50}{58.52} = 0.854$$

$\eta = 0.85$	/ 2 pt.

Q26: LOSS TOOL

Modify the converter data input parameters in the provided loss tool in MATLAB and run it to acquire the losses for the different values of U_{in} and P_{out} (the loss tool already includes these values and performs the necessary simulations). Read the comments in the code carefully to obtain valid results.

From these results, identify the nominal operating point and compare it with your results; It may be different from your calculation since the losses are calculated with the pessimistic approximation of switching losses. Additionally, give a brief explanation for why there are more or fewer losses for different operating conditions.

Initially, running the provided Loss Tool with our selected MOSFET (Type 6: Nexperia PHP18NQ11T) resulted in unexpectedly massive switching losses and negative efficiencies. After investigating with the course TAs, we confirmed that these results came from the way the tool handles the reverse recovery charge (Q_{rr}).

Since we are assuming perfect Zero Volt Switching (ZVS), the diodes turn off softly, effectively eliminating reverse recovery losses. The tool, however, used the pessimistic hard-switching approximation injecting over 1 W of loss per transistor ($\star$) . Furthermore, the library file incorrectly had $Q_{rr} = 0$ for Types 1, 2, and many others which gave them an unrealistic advantage in the simulations.

So, we modified the *DeviceLibrary_2026.mat* to set the Q_{rr} of type 6 transistor to 0 to remove turn on losses from the graph. In that manner, we see that the obtained result match our calculations. This also allows us to comper type 6 transistor with type 1 and 2, showing similar results.

In addition, we changed the efficiency formula in the Loss Tool (to obtain figure 16 and figure 17) to match with our previous question.
($\star$) $P_{rr,pri} = V_{ds} \times Q_{rr} \times freq = 60 \times 135 \times 10^{-9} \times 250'000 = 2.03\text{W}$, $P_{rr,sec} = V_{ds} \times Q_{rr} \times freq = 24 \times 135 \times 10^{-9} \times 250'000 = 0.81\text{W}$
$P_{rr,tot} = 4P_{rr,pri} + 4P_{rr,sec} = 11.3\text{W}$
$\Rightarrow$ These values match the ones found by the simulation.

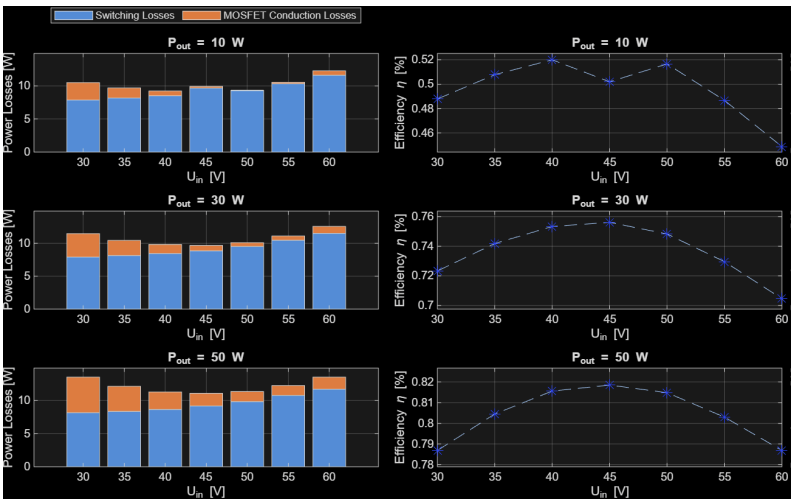


Figure 16 Semiconductor power losses with the simulation set with type 6 transistors.

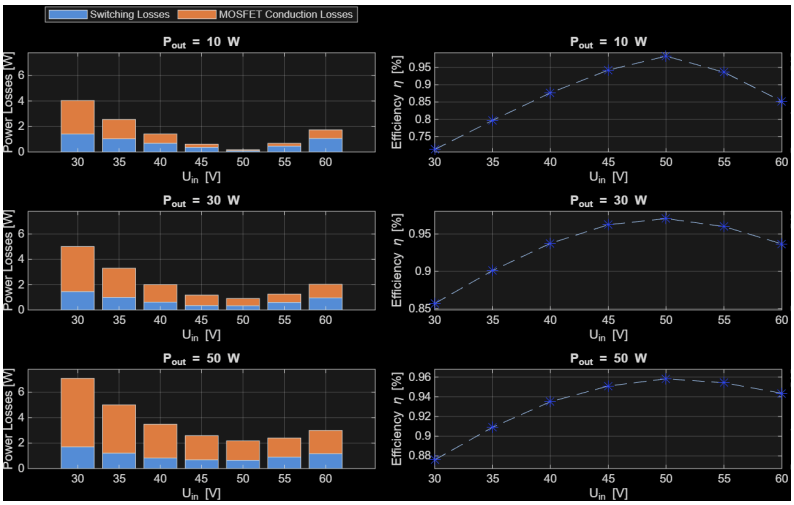


Figure 17 Semiconductor power losses with the simulation set with type 6 transistors and Q_{rr} set to 0

In the second simulation (with the $Q_{rr} = 0$), we found indeed that the worst efficiency at 50 W is around 88%, which is close to the efficiency found in Q25 (that was an impossible worst case, so it is normal to have a slightly higher efficiency).

We observe that varying U_{in} changes the losses. In Q23 adn Q24, we observed that the switching losses were larger in the primary side at 60 V, and that they were larger in the secondary side at 30 V, thus explaining the "U" shape in the switching losses (The loss starts decreasing, stabilizes for U_{in} around 45/50 V then starts increasing again).

We also observe that the efficiency is lower at smaller P_{out}, this is because the switching losses stay almost constant at different P_{out} thus having higher impact at lower P_{out}.

Finally, we observe that the highest efficiency is achieved at $U_{in} = 50$ V, which is our nominal input voltage.

/ 4 pt.

***NOTE**: You may consider not using a heatsink for the transistor and/or diode. Nevertheless, your decision should be based on your calculations and factors considered (i.e., temperature margin).*

Q27: PRIMARY SIDE HEATSINK SELECTION

To choose a proper heatsink, answer the following questions. For the calculations, assume a maximum ambient temperature of $\vartheta_a = 40\,°C$, whereas the semiconductor junction temperature should not exceed $\vartheta_j = 135\,°C$.

NOTE: There is already a thermal resistance from the junction to the case of the semiconductor. This can be found on the MOSFETs' data sheets.
NOTE: Since the MOSFETs have an exposed drain on the backside, a thermally conductive insulating (TIM) sheet is required for electrical isolation. The thermal resistance of the TIM sheet is assumed to be $3\,°C\,W^{-1}$.

a) Considering the output of the previous questions, determine the worst case operation condition for the primary side MOSFET in terms of power losses $P_{Q,pri}|_{wc}$.
b) Calculate the maximum allowed heatsink thermal resistance $R_{th,Q,pri,c-a}$ (where $_{c-a}$ indicates case to ambient).
c) Based on b), choose a heatsink from the selection provided in Table 3, their profile is also displayed in Fig. 18. Don't forget to highlight your selection in blue, as in Table 2.
d) Once the heatsink is selected, give the expected maximum junction temperature.

a) $P_{Q,pri}|_{wc} = P_{cond} + P_{switch} = 0.26 + 0.39 = 0.65$ W
b) The maximum allowed total thermal resistance from junction to ambient is:

$$R_{th,j-a,max} = \frac{\vartheta_j - \vartheta_a}{P_{Q,pri}|_{wc}} = \frac{135 - 40}{0.65} = 146.15\ \text{K/W}$$

From the datasheet, the junction-to-case thermal resistance is $R_{th,j-c} = 1.9$ K/W. Therefore, the maximum allowed case-to-ambient thermal resistance is:

$$R_{th,Q,pri,c-a} = R_{th,j-a,max} - R_{th,j-c} = 146.15 - 1.9 = 144.25\ \text{K/W}$$

(Note: If a heatsink were used, it would need a rating of $144.25 - 3 = 141.25$ K/W to account for the TIM sheet).
c) From the datasheet, the thermal resistance of the bare package in free air is $R_{th,j-a,bare} = 60$ K/W. Since 60 K/W is significantly lower than the total allowed 146.15 K/W, the package dissipates heat sufficiently on its own. We choose to not put any heatsink.
d) $\vartheta_{Q,pri,j,max} = \vartheta_a + P_{Q,pri}|_{wc} \times R_{th,Q,pri,j-a} = 40 + 0.65 \times 60 = 79^{\circ}C$

"Practical Design Note" :
Assuming our converter does not achieve ZVS, we can add the P_{rr} (see (★) Q26) to estimate an even worse case. In the case of primary side, we need to add $P_{rr,pri} = 2.03$ W of power, this increases the dissipated power to $P_{Q,pri}|_{wc} = 3.68$ W. Then the calculation becomes :

$$R_{th,j-a,max} = \frac{\vartheta_j - \vartheta_a}{P_{Q,pri}|_{wc}} = \frac{135 - 40}{3.68} = 25.8\ \text{K/W}$$

This does not allow the transistor to be left without an heatsink.

- If we use a type 4 heatsink per transistor :

$$R_{th,Q,pri,j-a} = 10.4 + 1.9 + 3 = 15.3\ \text{K/W}$$

$$\vartheta_{Q,pri,j,max} = \vartheta_a + P_{Q,pri}|_{wc} \times R_{th,Q,pri,j-a} = 40 + 3.68 \times 15.3 = 96^{\circ}C$$

- If we use a type 3 heatsink per transistor :

$$R_{th,Q,sec,j-a} = 7.5 + 1.9 + 3 = 12.4\ \text{K/W}$$

$$\vartheta_{Q,pri,j,max} = \vartheta_a + P_{Q,pri}|_{wc} \times R_{th,Q,pri,j-a} = 40 + 3.68 \times 12.4 = 86^{\circ}C$$

Both heatsinks allow to keep the transistors safely below the 135°C limit, even if ZVS is lost.

$P_{Q,pri}\|_{wc}$ = 0.65 W	$R_{th,Q,pri,c-a}$ = 144.25 K W^{-1}	
MOSFET heatsink model No. -	$\vartheta_{Q,pri,j,max}$ = 79 °C	/ 8 pt.

Q28: SECONDARY SIDE HEATSINK SELECTION

Similar to the primary side, a secondary side heatsink has to be selected. Assuming the same thermal constraints, answer the following questions:
NOTE: There is already a thermal resistance from the junction to the case of the semiconductor. This can be found on the MOSFETs' data sheets.
NOTE: Since the MOSFETs have an exposed drain on the backside, a thermally conductive insulating (TIM) sheet is required for electrical isolation. The thermal resistance of the TIM sheet is assumed to be 3 °C W^{-1}.

a) Considering the output of the Loss Tool, determine the worst case operation condition for the diode in terms of losses $P_{Q,sec}|_{wc}$.
b) Calculate the maximum allowed heatsink thermal resistance $R_{th,Q,sec,c-a}$.
c) Select a suitable heatsink from the selection provided in Table 3 (this time highlight it in green).
d) Give the expected maximum junction temperature.

a) $P_{Q,sec}|_{wc} = P_{cond} + P_{switch} = 1.12 + 0.36 = 1.48$ W
b) With the same reasoning as before :

$$R_{th,j-a,max} = \frac{\vartheta_j - \vartheta_a}{P_{Q,sec}|_{wc}} = \frac{135 - 40}{1.48} = 64.2 \text{ K/W}$$

$$R_{th,Q,sec,c-a} = R_{th,j-a,max} - R_{th,j-c} = 64.2 - 1.9 = 62.3 \text{ K/W}$$

c) From the datasheet, the bare package thermal resistance is $R_{th,j-a,bare} = 60$ K/W. While this is technically lower than the required 64.19 K/W, it leaves a dangerously small safety margin (This results in a junction temperature of approx 129°C). To ensure reliable operation without over-engineering the cooling system, we select a moderate heatsink: Ohmite EA-T220-38E (Model No. 4). It has a thermal resistance of 10.4 K/W and is designed to accommodate two devices, allowing us to cool the entire H-bridge with just two heatsinks.
d) Because the heatsink is shared between two transistors, it must dissipate the power of two MOSFETs: $P_{Q,sec}|_{total} = 2 \times 1.48 = 2.96$ W. However, the heat flowing through the individual TIM sheet and device case remains 1.48 W.
The expected maximum junction temperature is calculated as the ambient temperature, plus the temperature rise of the shared heatsink, plus the temperature rise across the individual TIM and case:

$$\vartheta_{Q,sec,j,max} = \vartheta_a + \left(P_{Q,sec}|_{total} \times R_{th,HS}\right) + \left(P_{Q,sec}|_{wc} \times (R_{th,TIM} + R_{th,j-c})\right)$$

$$\vartheta_{Q,sec,j,max} = 40 + (2.96 \times 10.4) + 1.48 \times (3 + 1.9) = 40 + 30.78 + 7.25 = 78.0°\text{C}$$

"Practical Design Note" :
Assuming our converter does not achieve ZVS, we can add the P_{rr} (see (★) Q26) to estimate an even worse case. In the case of secondary side, we need to add $P_{rr,sec} = 0.81$ W of power, this increases the dissipated power to $P_{Q,sec}|_{wc} = 2.29$ W.Then the calculation becomes :

$$R_{th,j-a,max} = \frac{\vartheta_j - \vartheta_a}{P_{Q,sec}|_{wc}} = \frac{135 - 40}{2.29} = 41.48 \text{ K/W}$$

This does not allow the transistor to be left without an heatsink. Let's us one type 4 heatsink per transistor to cool it down :

$$R_{th,Q,sec,j-a} = 10.4 + 1.9 + 3 = 15.3 \text{ K/W}$$

- If we maintain our design choice of using the shared Type 4 heatsink for the H-bridge, the junction temperature under this extreme hard-switching condition would be:

$$\vartheta_{Q,sec,j,max} = \vartheta_a + (2 \times 2.29 \times 10.4) + 2.29 \times (3 + 1.9) = 40 + 47.63 + 11.22 = 98.9°\text{C}$$

- If we decide to use one heatsink per transistor :

$$\vartheta_{Q,sec,j,max} = \vartheta_a + P_{Q,sec}|_{wc} \times R_{th,Q,sec,j-a} = 40 + 2.29 \times 15.3 = 75.0°\text{C}$$

This proves that in both cases, the method is robust enough to keep the transistors safely below the 135°C limit, even if ZVS is completely lost.

$P_{Q,sec}\big\vert_{wc}$ = 1.48 W	$R_{th,Q,sec,c-a}$ = 62.3 K W^{-1}	
MOSFET heatsink model No. : 4	$\vartheta_{Q,sec,j,max}$ = 78 °C	/ 8 pt.

Table 3 List of the offered heatsinks.

No.	Manufacturer	Product	R_{th} (K W^{-1})	Figure
1†	Ohmite	FA-T220-64E	3.00	18a
2†	Ohmite	FA-T220-25E	4.70	18a
3†	Ohmite	EA-T220-51E	7.50	18b
4†	Ohmite	EA-T220-38E	10.40	18b
5	Ohmite	OMNI-220-18-25-1C	3.50	18b
6†	Ohmite	OMNI-220-18-50-2C	7.00	18b

†: You can use this heatsink for 2 devices.

(a) Ohmite FA-T220-xxE (b) Ohmite EA-T220-xxE (c) Wakefield 693-xxx

Figure 18 Available heatsinks. Images taken from the manufacturer websites.

REPORT 1 SUMMARY

Fill out the table below with your results as well as your chosen devices:

Table 4 Calculated parameter values, selected components and efficiency.

Property	Value	Unit
N	$2.08 = \frac{25}{12}$	—
C_{in}	1.62	µF
L	8.33	µH
$C_{DCBLOCK}$	4.86	µF
C_{out}	6.12	µF
Primary side MOSFET No.	6	—
Secondary side MOSFET No.	6	—
$\eta\|_{nom}$	86	%
Primary side MOSFET heatsink No. (if present)	-	—
Secondary side MOSFET heatsink No. (if present)	4	—

Total: **/ 125 pt.**